ngvla
Next Generation Very Large Array

Reference Design Antenna Electronics

Jim Jackson, NRAO

NSF AUI NRAO

Requirements

- Front Ends
  - 70 – 116 GHz
  - 30.5 – 50.5 GHz
  - 20.5 – 34.0 GHz
  - 12.3 – 20.5 GHz
  - 3.5 – 12.5 GHz
  - 1.2 – 3.5 GHz
  - Cooled to 20K

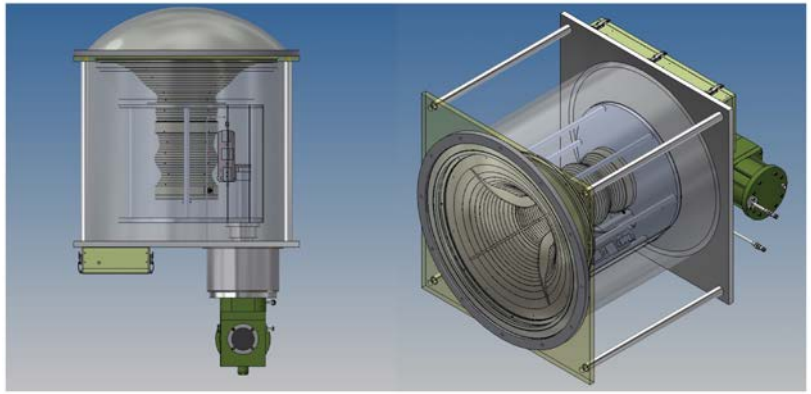
- Antennas: 263 total
  - Main Array: 214, 18m
  - Long Baseline: 30, 18m
  - Total Power: 19, 6m
  - **~10x VLA**
- Operating Cost: **~3x VLA**
  - Reduced Power Cost
  - Reduced Maintenance Cost

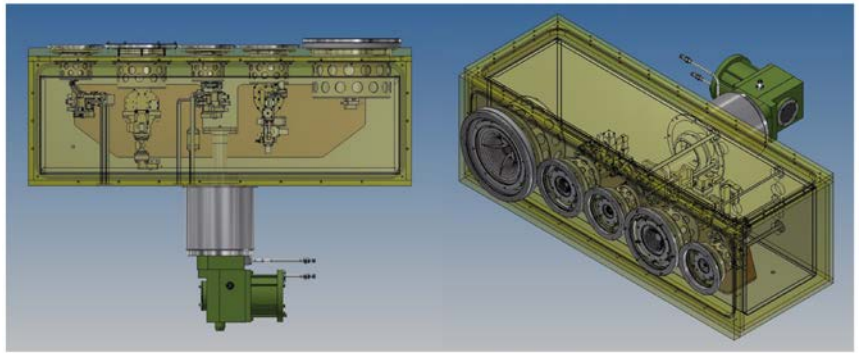
Design Philosophies

- Utilize highly integrated, easily manufacturable sub-assemblies
- Minimize number of Line Replaceable Units (LRUs)
- Emphasize low power, high reliability designs
- Provide advanced remote diagnostic & fault prediction capability
  - Know which LRU has failed before visiting an antenna: swap & return
  - Predict what's about to fail to better schedule maintenance visits
- Focus on an efficient and reliable cryogenic system
  - Current cryogenic designs dominate VLA power and maintenance
- Digitize as close as possible to the front ends
  - Minimizes use of less reliable components
    - Analog electronics – require frequent calibration and attention
    - Mechanical switches – high failure items in VLA and VLBA

Front Ends / Dewars

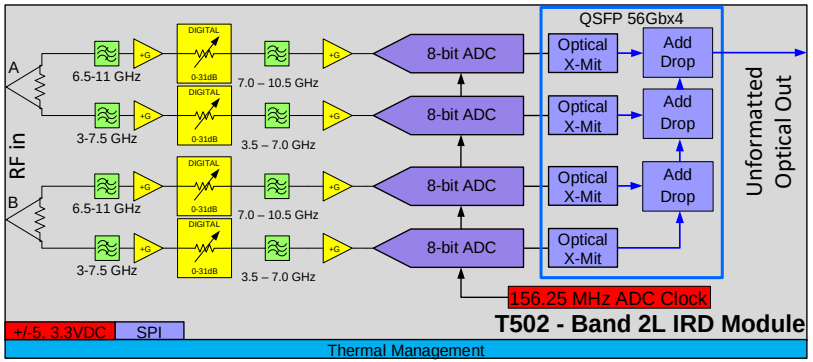
- 6 receivers in 2 dewars
  - Covering 1.2 – 116 GHz
  - Compact, cooled feeds
  - Linear polarization
  - Total mass ~120 Kg
  - RF output at sky frequency
- Upcoming presentation by: Denis Urbain, NRAO

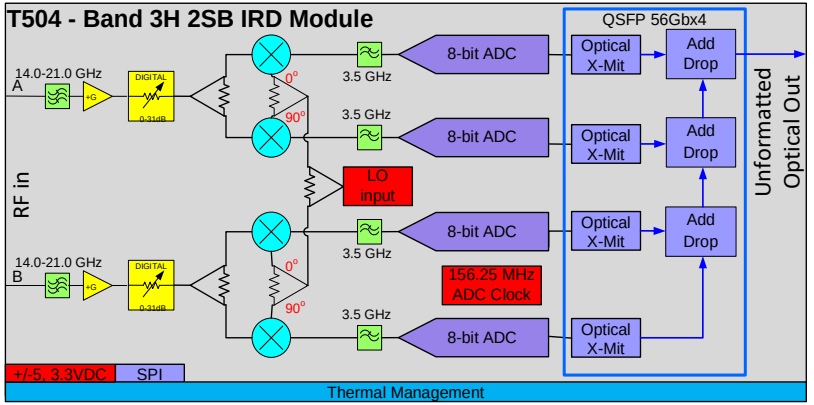




Integrated Downconverters / Digitizers (IRD)

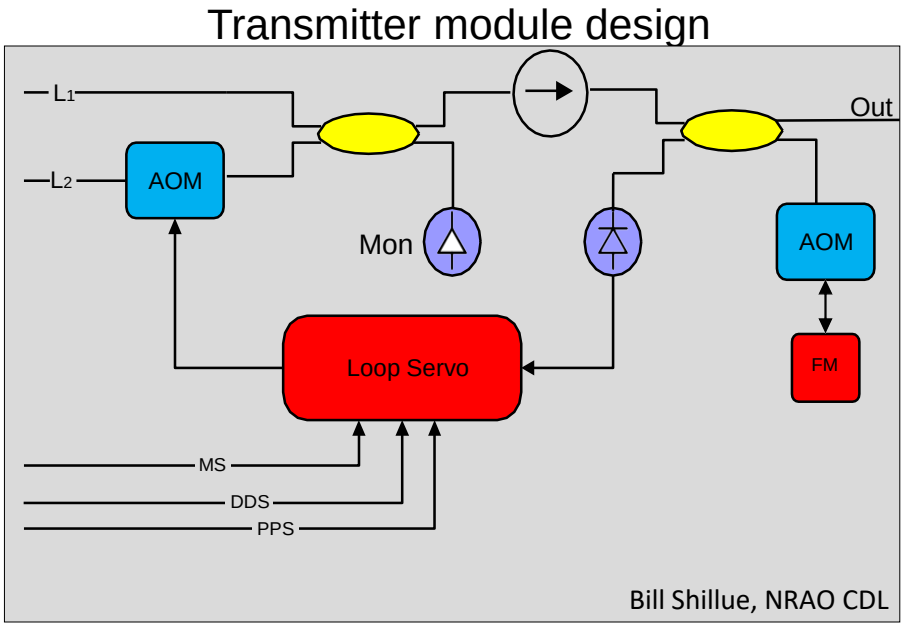
- Small integrated modules mounted at secondary focus near the front ends
- Direct sampling for 1.2 – 14 GHz
- Downconverted sideband separating sampling for 14 – 116 GHz
- Custom digitizer IC in development:
  - 8 bit, 7 Gsps for bands 1-5
  - 4 bit, 14 Gsps for band 6
- Output on multiple 56 Gbps unformatted optical data streams
- Upcoming detailed presentation by: Matt Morgan, NRAO CDL





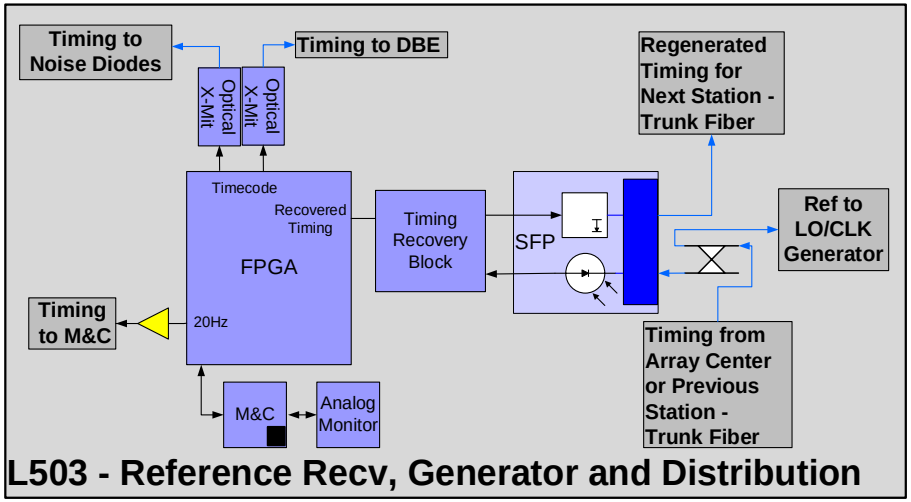
Central LO / Reference

- Based on SKA-mid design
  - Dual optical carrier transmission of reference & timing to antennas
    - L_1: Laser source
    - L_2: L_1 offset by 7 GHz + DDS
    - DDS offset is per antenna
  - 1 PPS embedded timing signal
  - Provides for round trip phase measurement



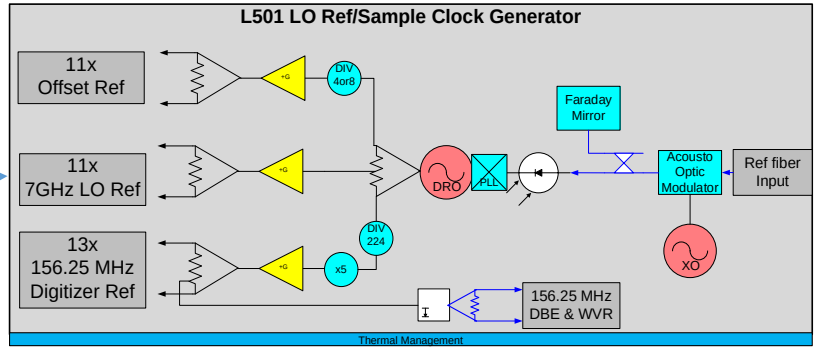
Reference & Timing Distribution

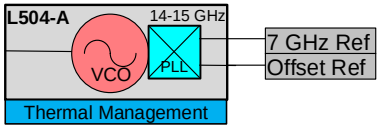
- Reference signals from array center are sent to two locations for timing recovery & local oscillator (LO) / sample clock generation
- **Pedestal rack:** PPS timing signal is recovered and used along with NTP in an FPGA to generate:
  - Timecode for Digital Back End (DBE)
  - Timing signal(s) for local M&C
  - Switching signal for front end noise diodes
  - Timing signal may also be regenerated for transmission to next station

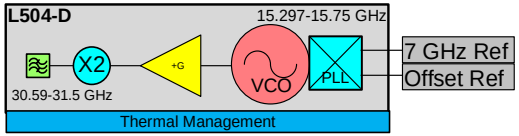


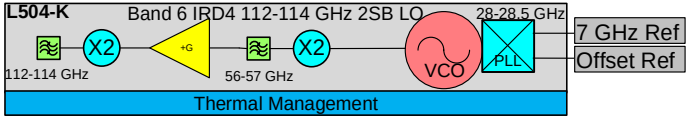
Local Oscillator & Clocks

- **Secondary Focus Enclosure:**
  - Reference generator:
    - Recovered signal locks 7 GHz reference oscillator
    - An offset reference is generated by dividing reference by 2, 4, or 8
    - 156.25 MHz digitizer clock reference
  - LO Modules:
    - Co-located with each 2SB IRD
    - Use 7GHz & offset reference to generated coarse tunable LO's for the mixers in the IRD modules









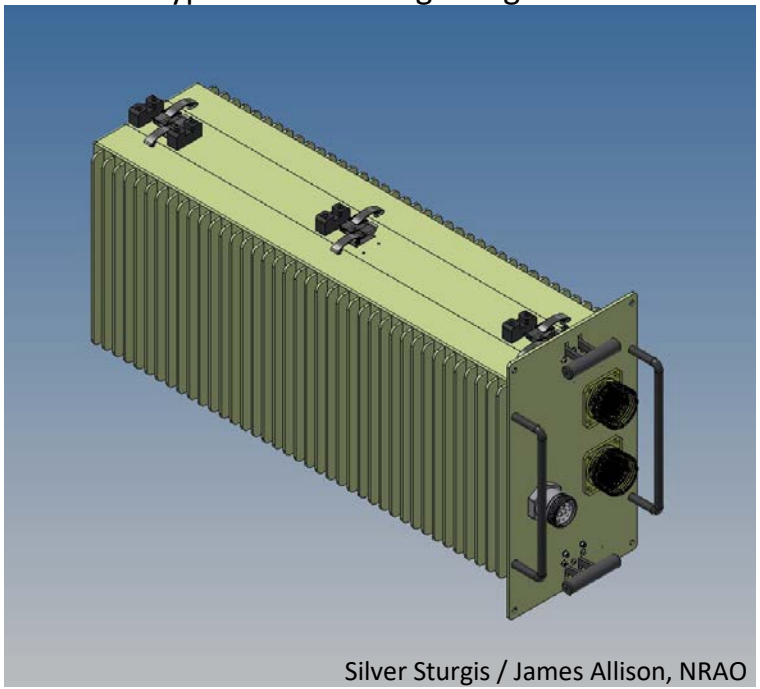
Cryogenics

- Large focus on cryogenic design
  - Lower power cost than VLA
  - Lower maintenance than VLA
- Current reference design is Gifford-McMann refrigerator & scroll compressor
  - Focus on improved technology & optimization of power consumption
  - Inverter based variable speed scroll compressors & refrigerators
  - Longer life components
  - Improved remote diagnostics for prediction & early detection of failures
- Testing of COTS and NRAO designed hardware in process in Socorro

Digital Back End / Data Transmission

- Highly integrated module
  - RFI tight sealed ARCS style module
  - Located in antenna pedestal
  - Circular multi-fiber connectors
  - Xilinx Virtex Ultrascale+ (VU29P) or similar FPGA w/ 58 Gbps SERDES
- **Data Input**: Unformatted 56 Gbps data links
  - received directly from IRD modules on fiber
- **Data Output**: 4x100 Gb Ethernet
  - To array center via owned fiber or commercial carrier

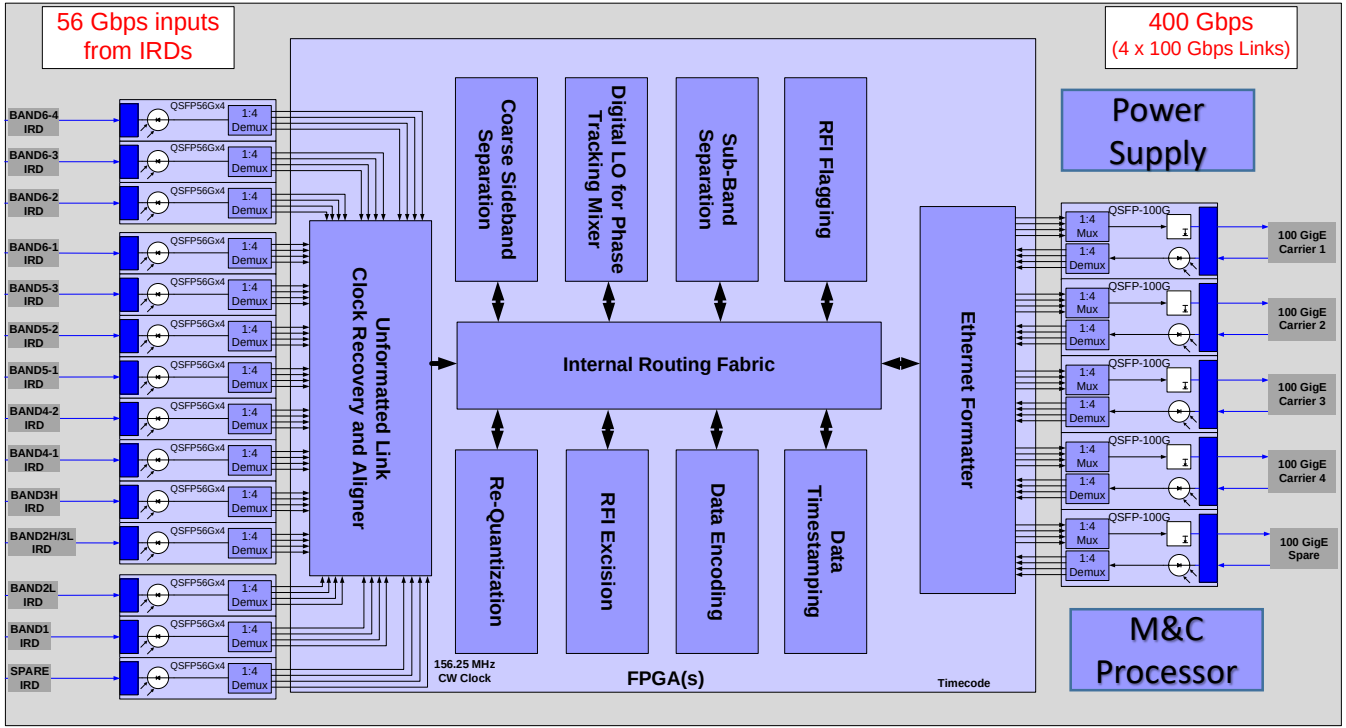
Prototype ARCS Housing Design for DBE



Silver Sturgis / James Allison, NRAO

Digital Back End / Data Transmission

- Block Diagram
  - Optical receivers
    - 56 Gbps, 4 lanes
  - Ethernet transceivers
    - 4x 100 GbE COTS
  - FPGA:
    - Xilinx Virtex Ultrascale+ (VU29P) or similar FPGA w/ 58 Gbps SERDES
  - Integrated M&C
    - Linux
  - -48V DC Power
    - Internal DC/DC converters
  - Timecode Input
    - Format TBD



Monitor & Control Hardware

- Local supervisor processor(s)
  - Manages local antenna functionality
  - Autonomous operation if not on M&C network
    - Safety & security functions
    - HVAC monitor & control
    - Power management
    - Recovery after outages
    - Local storage of monitor data
    - FPGA programming files
    - Hardware watchdog & resets
    - Local control by technicians during construction & maintenance visits
- Other antenna M&C functions
  - M&C Ethernet switch
  - Remote maintenance
  - 4 or 5 axis Antenna Control Unit (ACU)
  - Weather station (some antennas)
  - Individual module M&C functions
  - COTS hardware M&C functions
  - Security cameras
  - Fire / Intrusion alarms
  - VOIP telephones / Paging system

In Conclusion

- We have an electronics system that:
  - Meets published science requirements
  - Achieves desired operational cost goals
  - Represents a low risk design
  - Can be built utilizing current state of the art technology
- Utilized to generate realistic costing of the ngVLA reference design for the Decadal Submission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