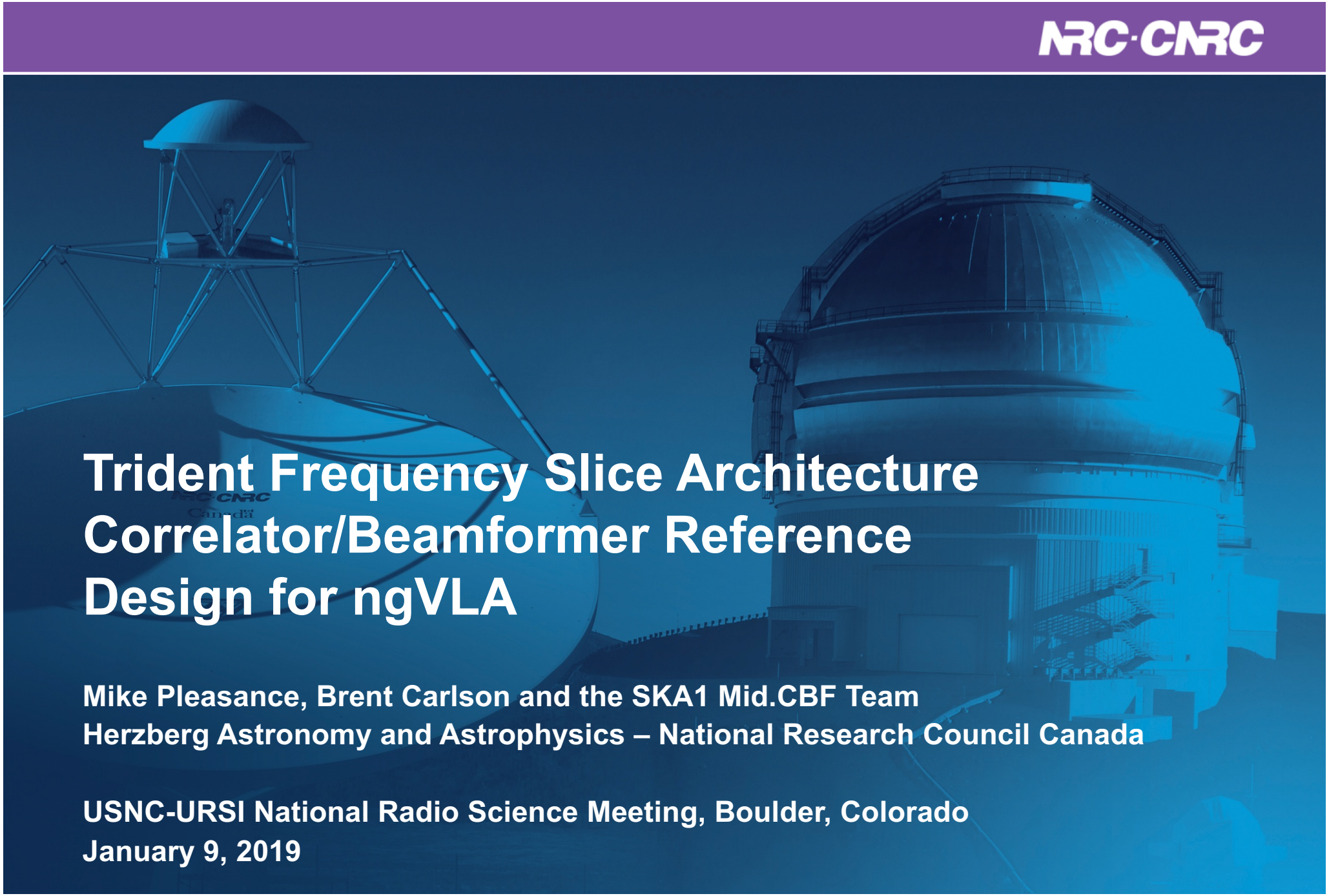


Trident Frequency Slice Architecture Correlator/Beamformer Reference Design for ngVLA

Mike Pleasance, Brent Carlson and the SKA1 Mid.CBF Team
Herzberg Astronomy and Astrophysics – National Research Council Canada

USNC-URSI National Radio Science Meeting, Boulder, Colorado
January 9, 2019

National Research Council Canada | Conseil national de recherches Canada

Canada

Outline

- ngVLA Correlator/Beamformer Requirements
- “Frequency Slice Architecture” Overview
- TALON-DX FPGA Board and TALON LRU
- Trident-CBF ngVLA CBF Design

ngVLA Correlator/Beamformer Key Requirements

- 263 dual-polarization antennas
- 20 GHz (per pol'n) instantaneous bandwidth for synthesis imaging
- Beamforming:
  - 10 pulsar timing beams
  - 10 pulsar search beams
  - 5 VLBI beams
- 28 GHz (per pol'n) aggregate bandwidth (simultaneous observing modes)
- Maximum baseline length of 10,000 km

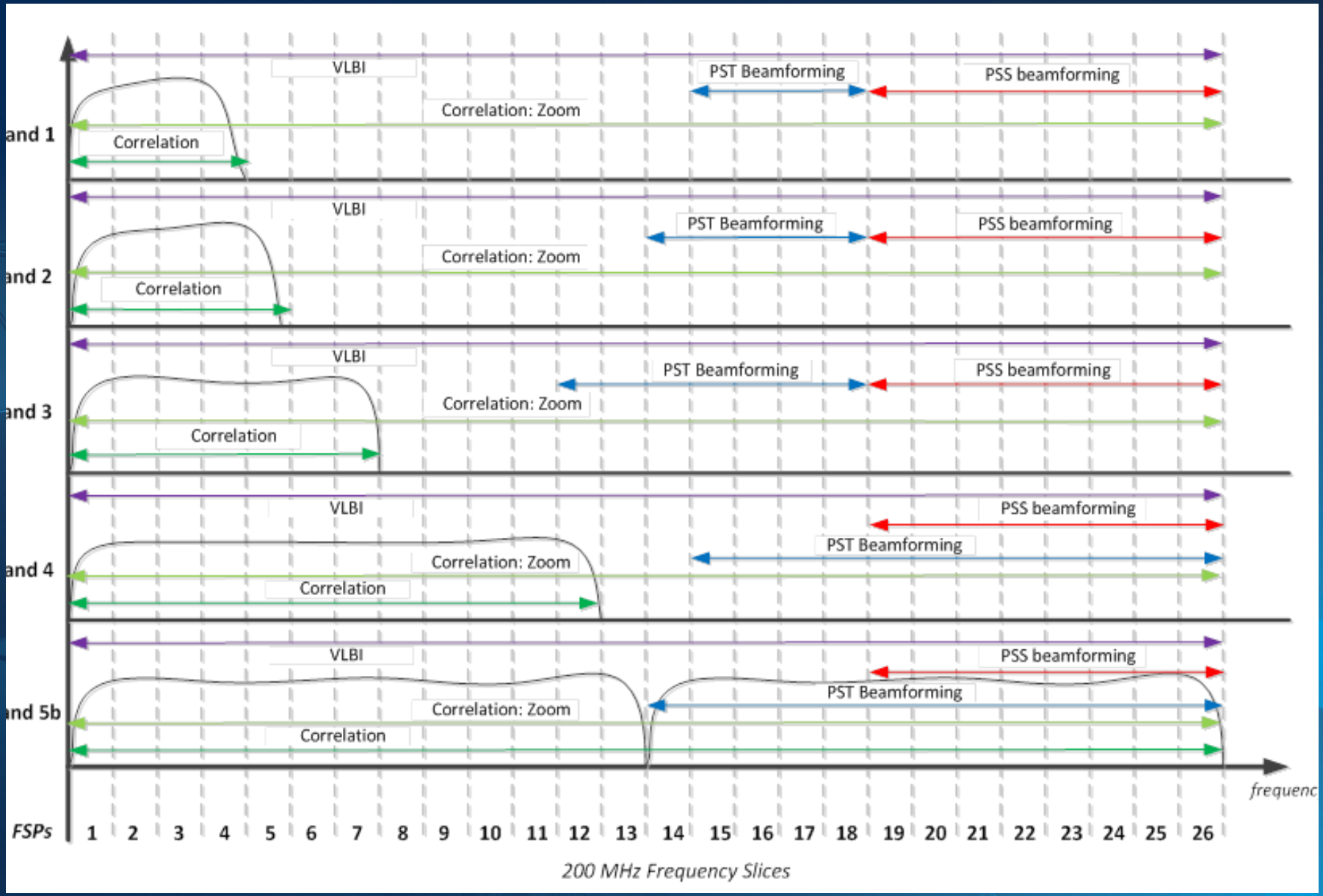
Frequency Slice Architecture -- Overview

- SKA1 Mid has 6 different Bands at 3 different sample rates
- Original design had full sub-arraying flexibility (anything in any sub-array) and many different FPGA designs to handle all of the Bands
- Frequency Slice Architecture, proposed to SKAO in early 2017:
  - Provides full bandwidth correlation/beamforming ability, but not everything at the same time and not *full* sub-array independence
  - Vastly reduced FPGA design effort
  - Dropped power and hardware by ~2X
  - Significant cost savings
- Accepted by SKAO and incorporated into SKA1 design baseline

Frequency Slice Architecture -- Overview

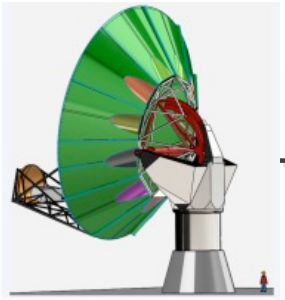
- In the “VCC”, split each digitized Band into 10/9 oversampled, equally-spaced, ~200 MHz “Frequency Slices”

- Process each Frequency Slice in a “Frequency Slice Processor” (FSP). Each (of 26) FSPs can do 1 thing (for SKA1 Mid):
  a. Correlation for imaging, w/ or w/o zoom, 16k channels
  b. Pulsar Search Beamforming (on tunable 300 MHz)
  c. Pulsar Timing Beamforming
  d. VLBI beamforming incl. 1k channel correlation for tied-array calibration solutions



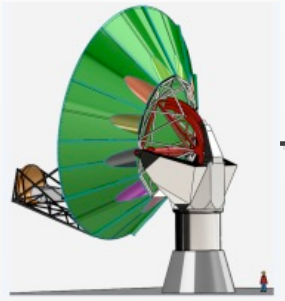
SKA1 Mid.CBF Frequency Slice/processing resources diagram

Frequency Slice Architecture -- Overview



Very Coarse Channelizer (VCC)

1



Very Coarse Channelizer (VCC)

2

263

200 MHz Frequency Slices

Function Mode-specific Frequency Slice Processor-1 (FSP-1)

Function Mode-specific Frequency Slice Processor-2 (FSP-1)

FSP-50

FSP-1 Data products

FSP-2 Data products

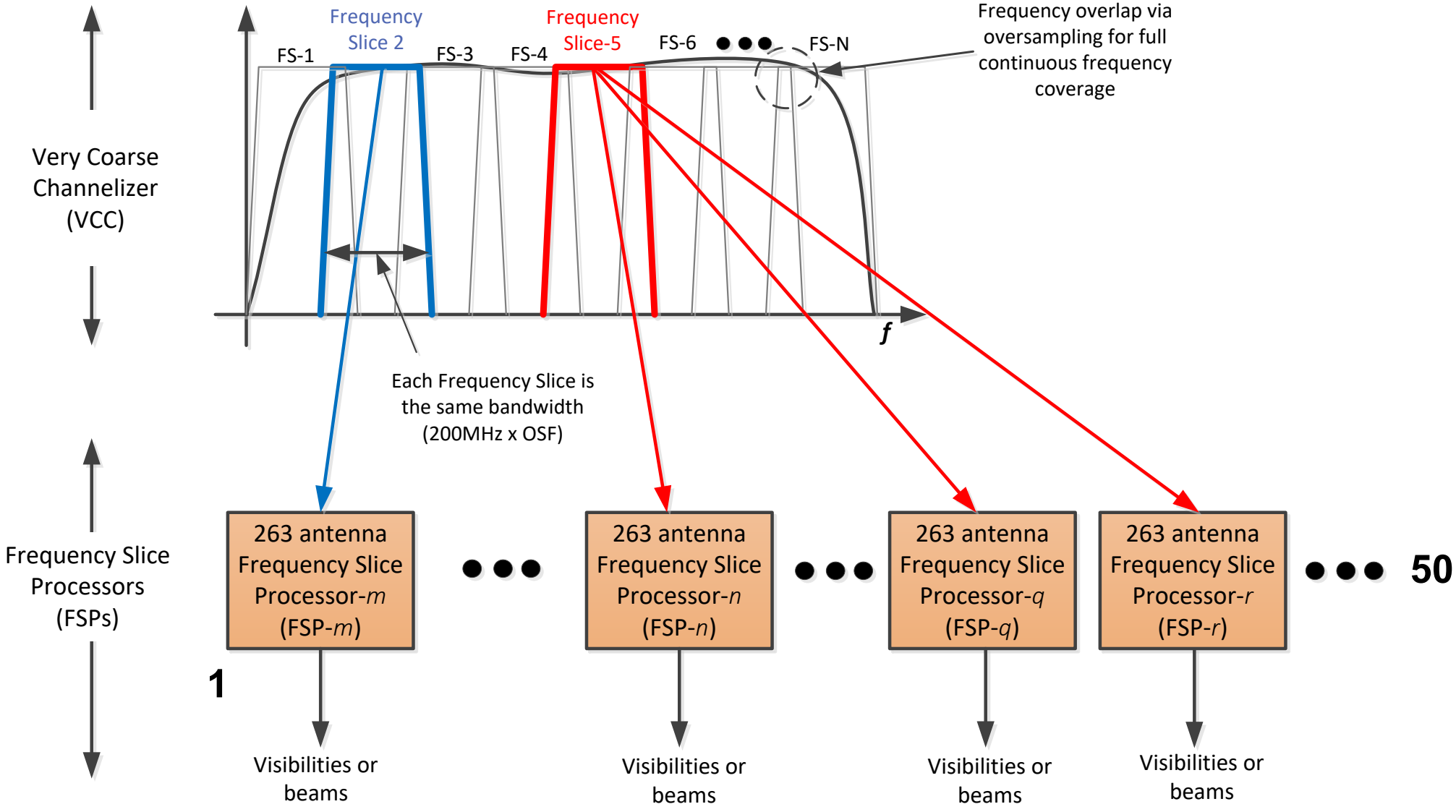
FSP-50 Data products

External Output Switch

Visibilities

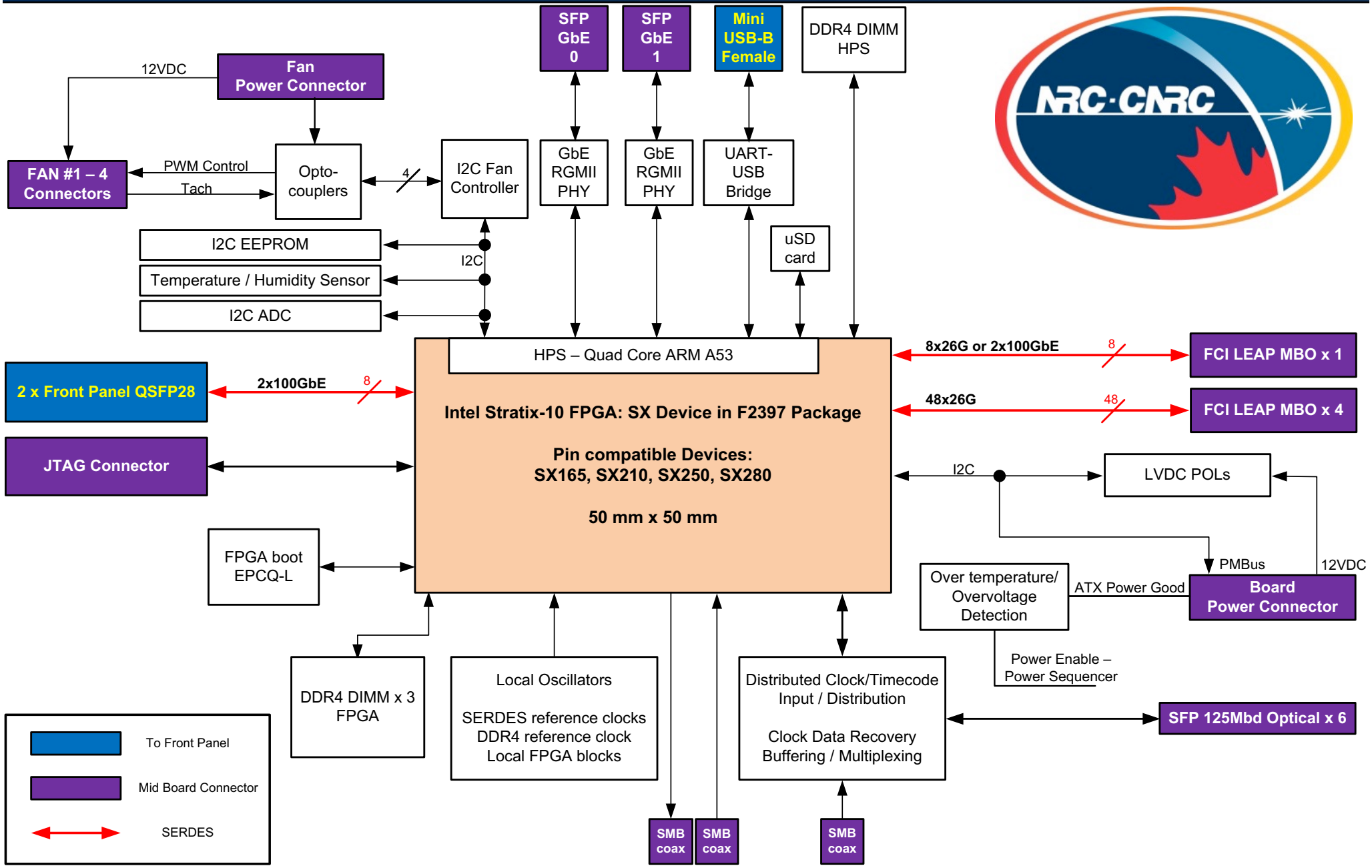
Phase-delay Beams

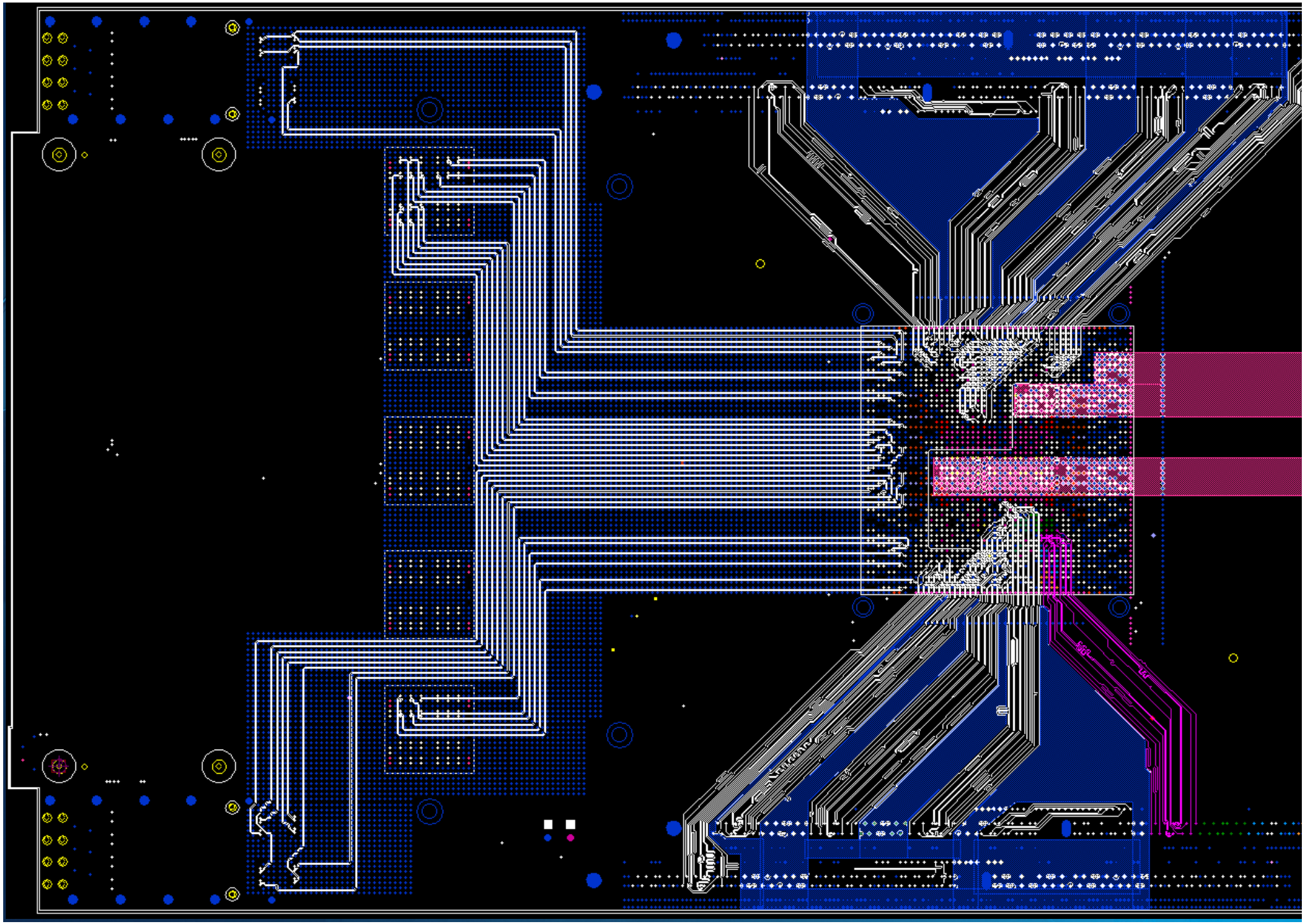
True-delay/ VLBI Beams

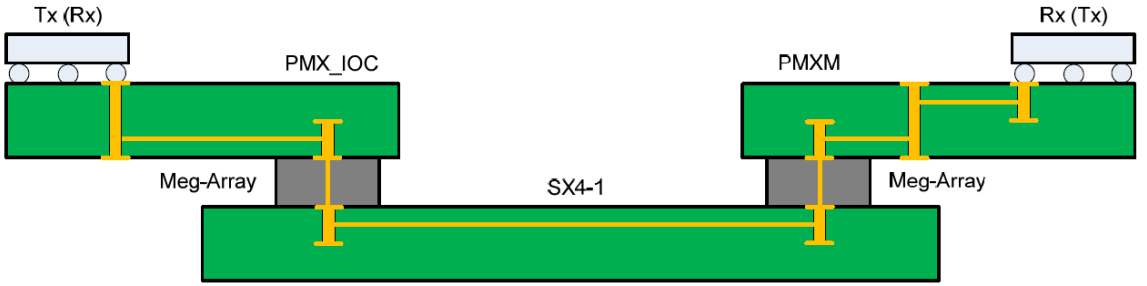

Very Coarse Channelizer (VCC)
Frequency Slice 2
Frequency Slice-5
FS-1
FS-3
FS-4
FS-6
FS-N
Frequency overlap via oversampling for full continuous frequency coverage
f
Each Frequency Slice is the same bandwidth (200MHz x OSF)
Frequency Slice Processors (FSPs)
263 antenna Frequency Slice Processor-m (FSP-m)
263 antenna Frequency Slice Processor-n (FSP-n)
263 antenna Frequency Slice Processor-q (FSP-q)
263 antenna Frequency Slice Processor-r (FSP-r)
1
50
Visibilities or beams
Visibilities or beams
Visibilities or beams
Visibilities or beams

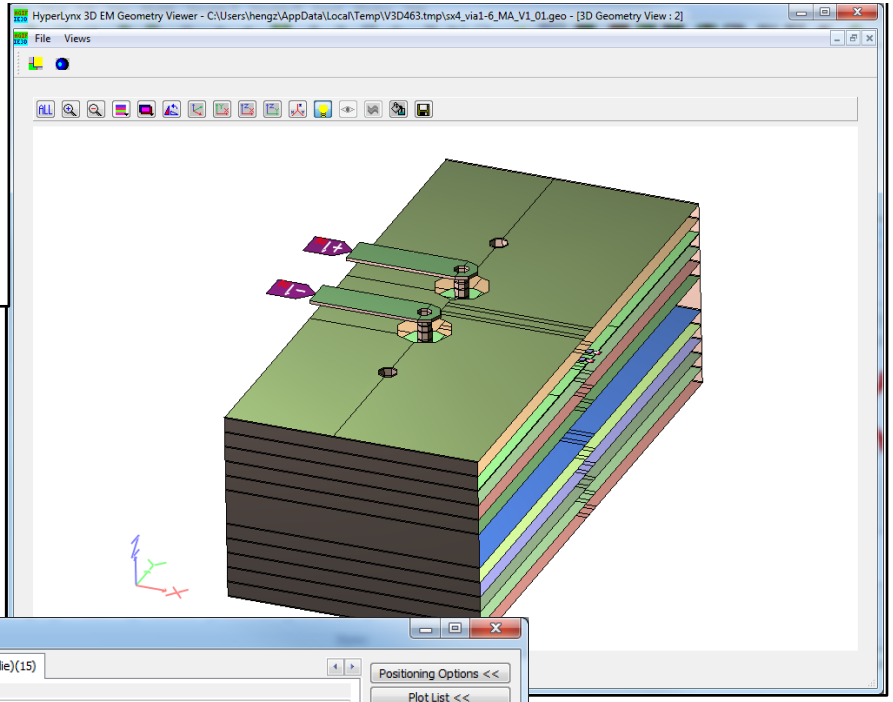
TALON-DX FPGA Board and TALON LRU

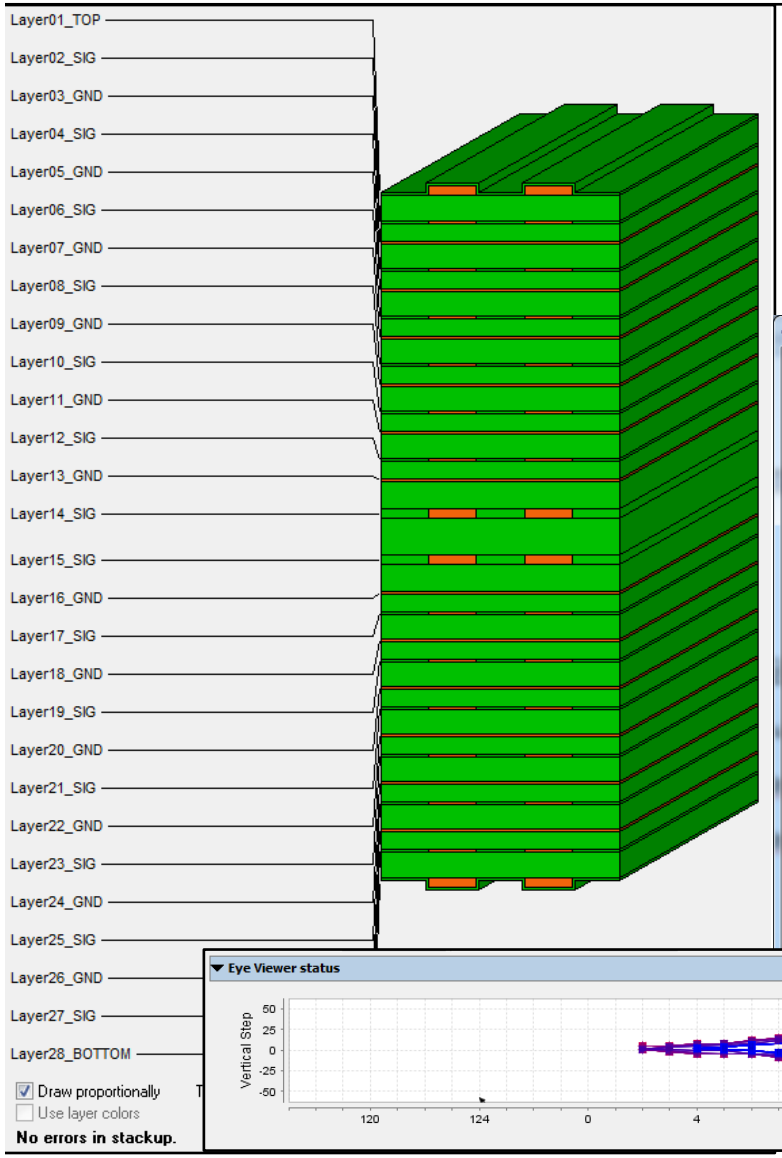
- Single Stratix-10 (14 nm FinFET) SX280 Intel FPGA on each “TALON-DX” board
- Embedded ARM processor in FPGA / 1 Gb Ethernet and for M&C
- 4 x DDR4 DIMMs (Single Rank: 2666 MT/s, Dual Rank: 2400 MT/s)
- 5 x 12 TRx FCI LEAP MBOs; 26G per fiber
- 2 x QSFP28 100G cages
- Air-cooled with stacked-fin heatsink
- 2 x TALON-DX boards in each 2U TALON LRU

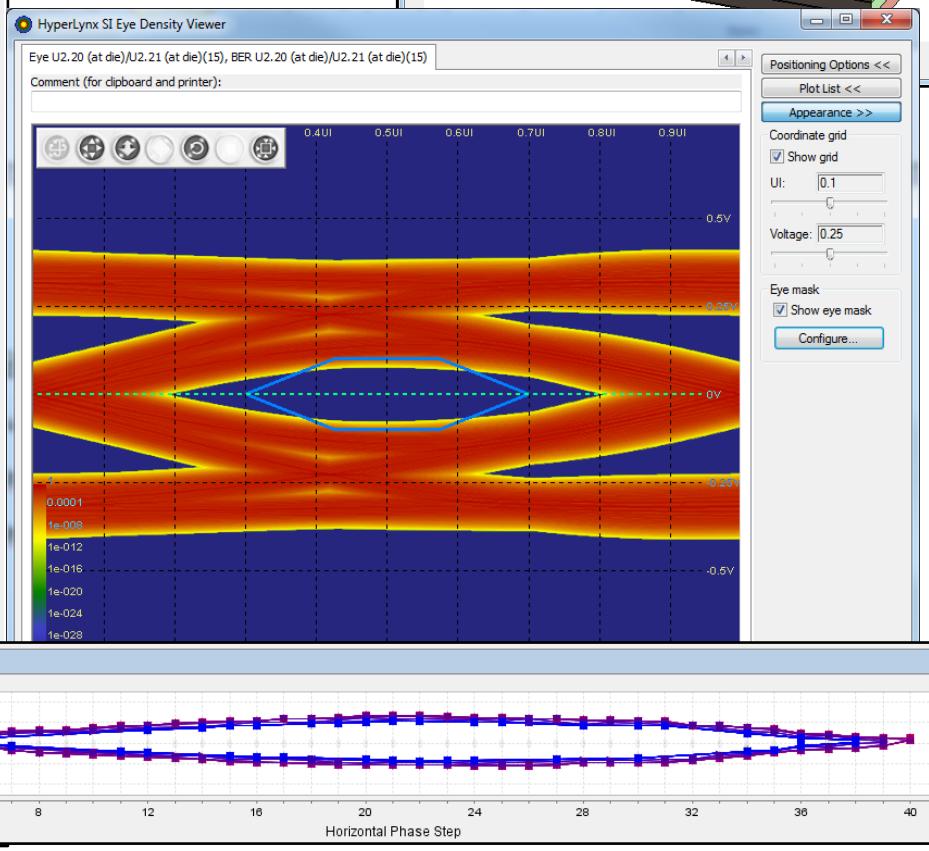

SFP GbE 0
SFP GbE 1
Mini USB-B Female
DDR4 DIMM HPS
12VDC
Fan Power Connector
FAN #1 – 4 Connectors
PWM Control
Tach
Opto-couplers
4
I2C Fan Controller
GbE RGMII PHY
GbE RGMII PHY
UART-USB Bridge
uSD card
I2C EEPROM
Temperature / Humidity Sensor
I2C ADC
I2C
HPS – Quad Core ARM A53
Intel Stratix-10 FPGA: SX Device in F2397 Package
Pin compatible Devices:
SX165, SX210, SX250, SX280
50 mm x 50 mm
2 x Front Panel QSFP28
2x100GbE
8
JTAG Connector
8x26G or 2x100GbE
8
FCI LEAP MBO x 1
48x26G
48
FCI LEAP MBO x 4
I2C
LVDC POLs
PMBus
12VDC
Over temperature/ Overvoltage Detection
ATX Power Good
Board Power Connector
Power Enable – Power Sequencer
FPGA boot EPCQ-L
DDR4 DIMM x 3 FPGA
Local Oscillators
SERDES reference clocks
DDR4 reference clock
Local FPGA blocks
Distributed Clock/Timecode Input / Distribution
Clock Data Recovery
Buffering / Multiplexing
SFP 125Mbd Optical x 6
SMB coax
SMB coax
SMB coax
To Front Panel
Mid Board Connector
SERDES

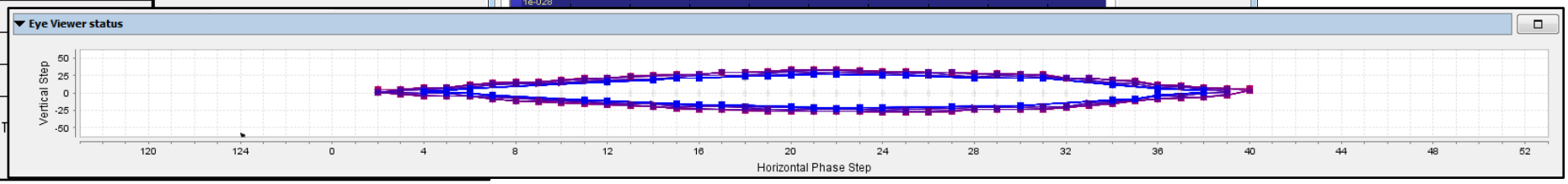


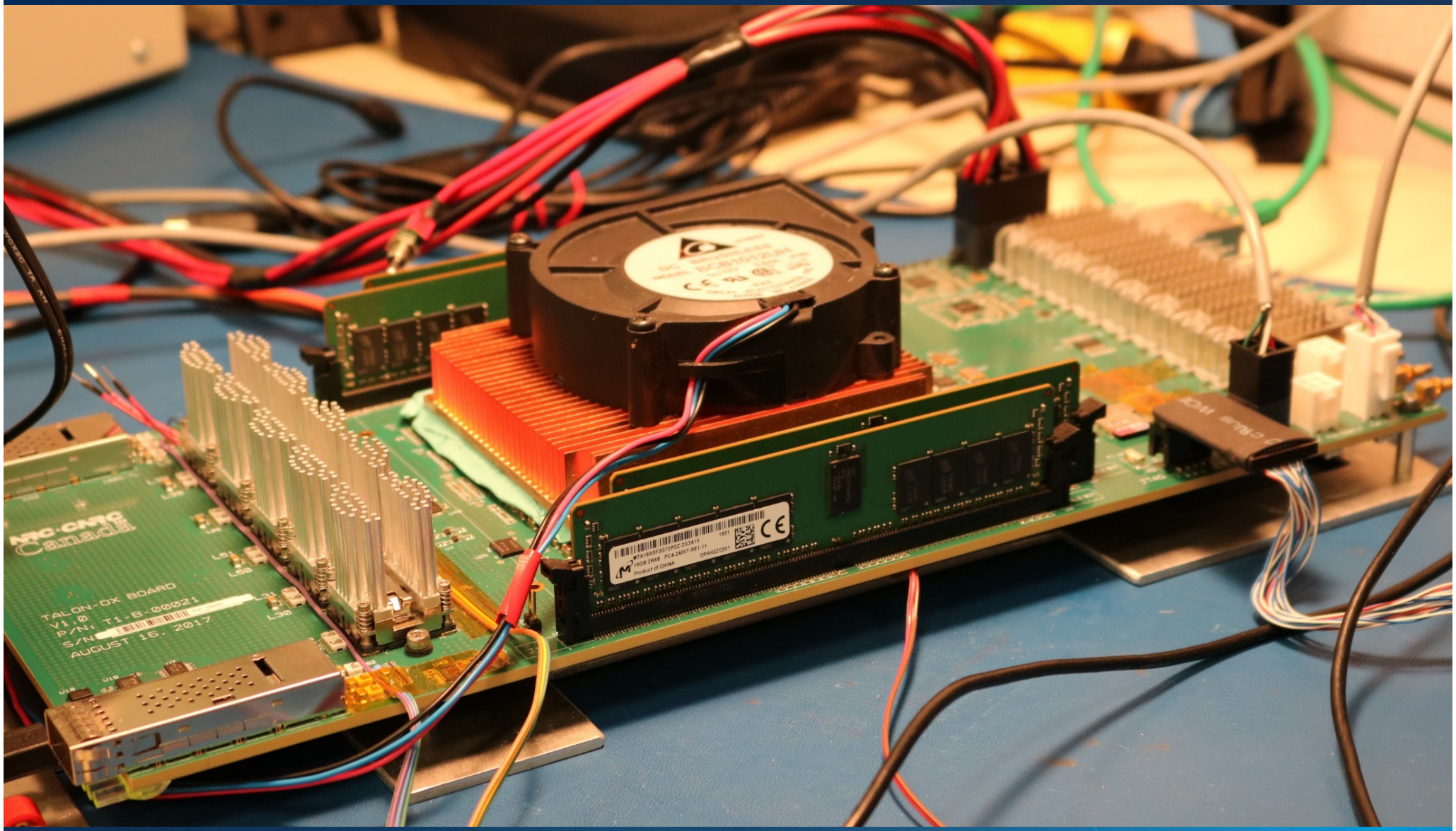

Tx (Rx)
Rx (Tx)
PMX_IOC
PMXM
Meg-Array
SX4-1
Meg-Array

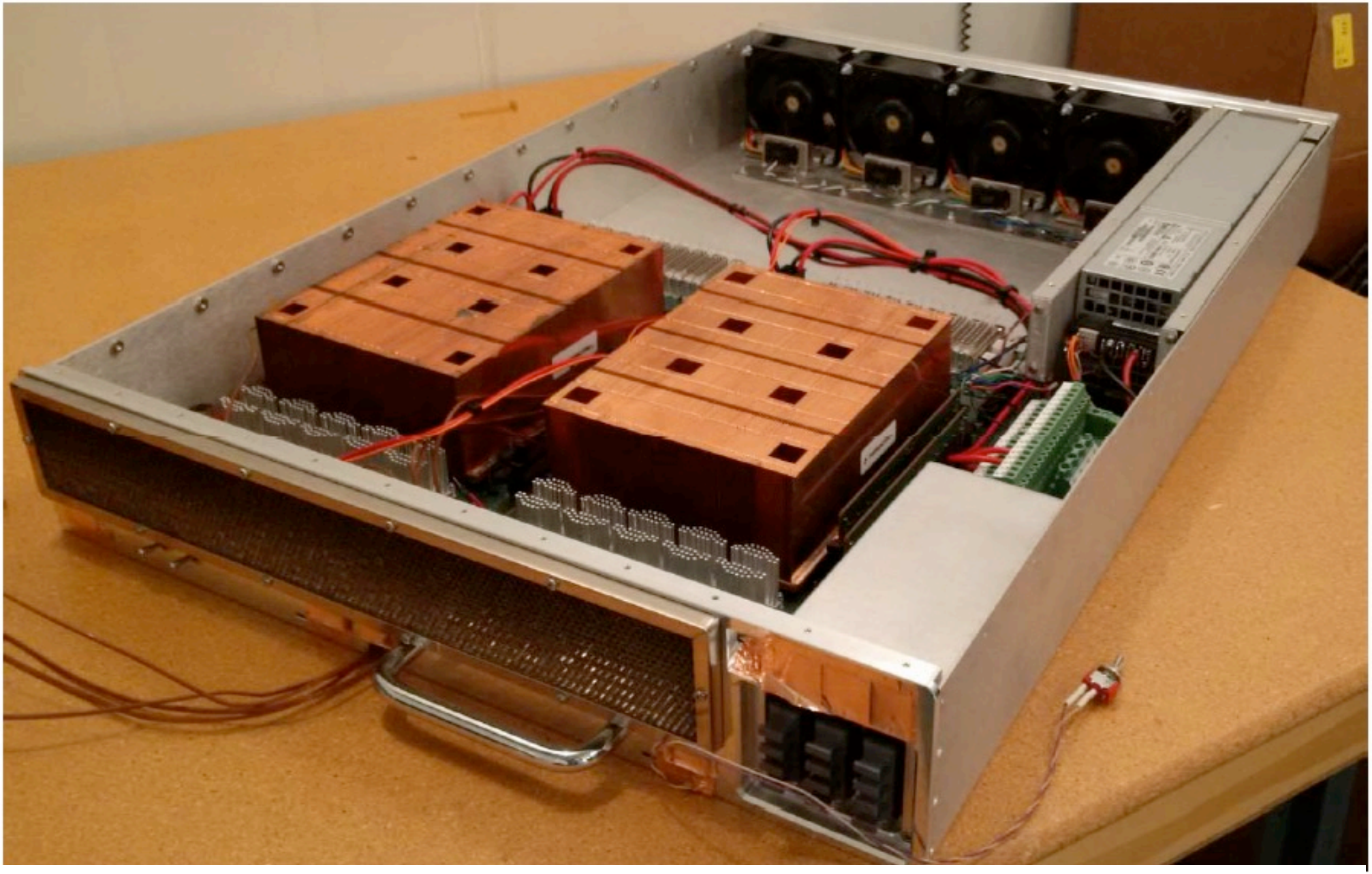

HyperLynx 3D EM Geometry Viewer - C:\Users\hengz\AppData\Local\Temp\V3D463.tmp\sx4_via1-6_MA_V1_01.geo - [3D Geometry View : 2]
File
Views


Layer01_TOP
Layer02_SIG
Layer03_GND
Layer04_SIG
Layer05_GND
Layer06_SIG
Layer07_GND
Layer08_SIG
Layer09_GND
Layer10_SIG
Layer11_GND
Layer12_SIG
Layer13_GND
Layer14_SIG
Layer15_SIG
Layer16_GND
Layer17_SIG
Layer18_GND
Layer19_SIG
Layer20_GND
Layer21_SIG
Layer22_GND
Layer23_SIG
Layer24_GND
Layer25_SIG
Layer26_GND
Layer27_SIG
Layer28_BOTTOM
Draw proportionally
Use layer colors
No errors in stackup.


HyperLynx SI Eye Density Viewer
Eye U2.20 (at die)/U2.21 (at die)(15), BER U2.20 (at die)/U2.21 (at die)(15)
Comment (for clipboard and printer):
Positioning Options <<
Plot List <<
Appearance >>
Coordinate grid
Show grid
UI: 0.1
Voltage: 0.25
Eye mask
Show eye mask
Configure...
0.4UI
0.5UI
0.6UI
0.7UI
0.8UI
0.9UI
0.5V
0V
-0.5V
0.0001
1e-008
1e-012
1e-016
1e-020
1e-024
1e-028


Eye Viewer status
Vertical Step
50
25
0
-25
-50
120
124
0
4
8
12
16
20
24
28
32
36
40
44
48
52
Horizontal Phase Step


NRC·CNRC
Canada
TALON-DX BOARD
V1.0
P/N: T1-B-00021
S/N
AUGUST 16, 2017

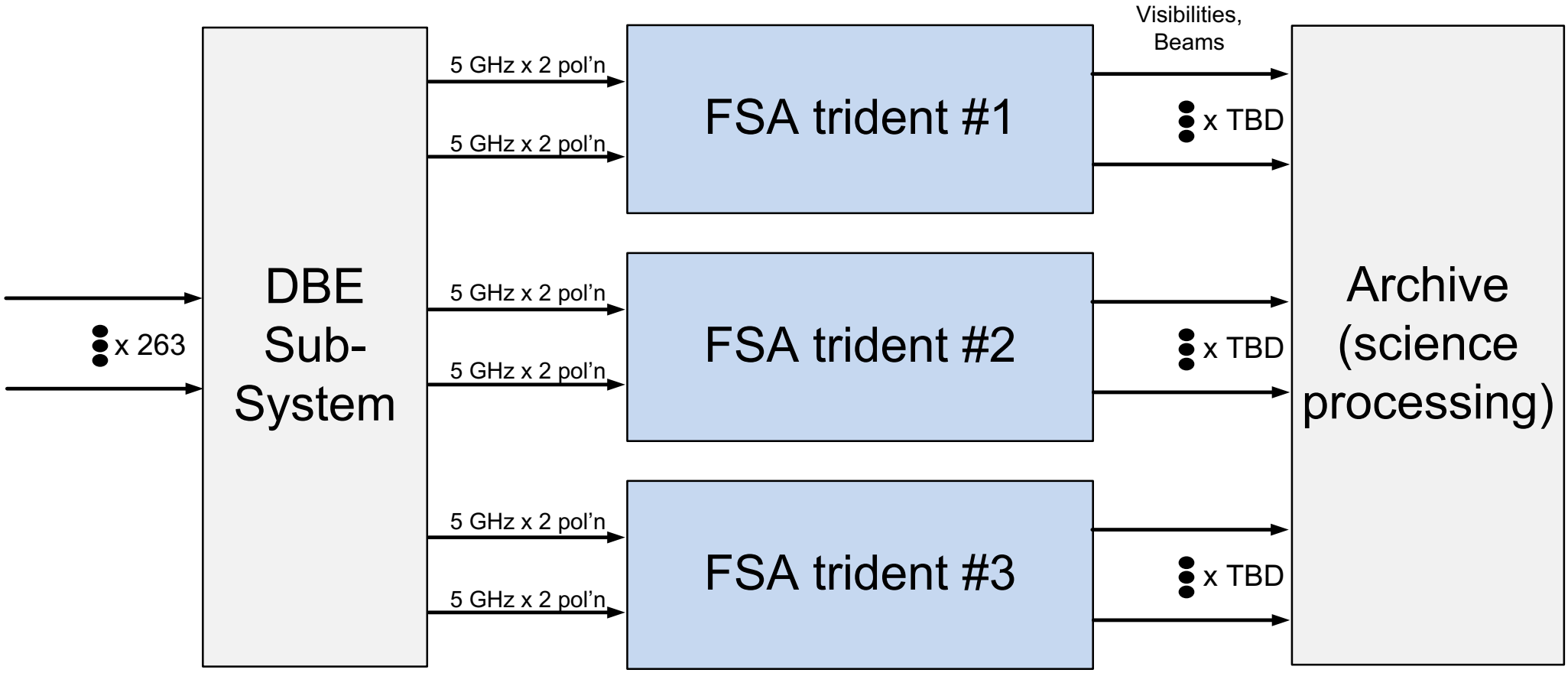


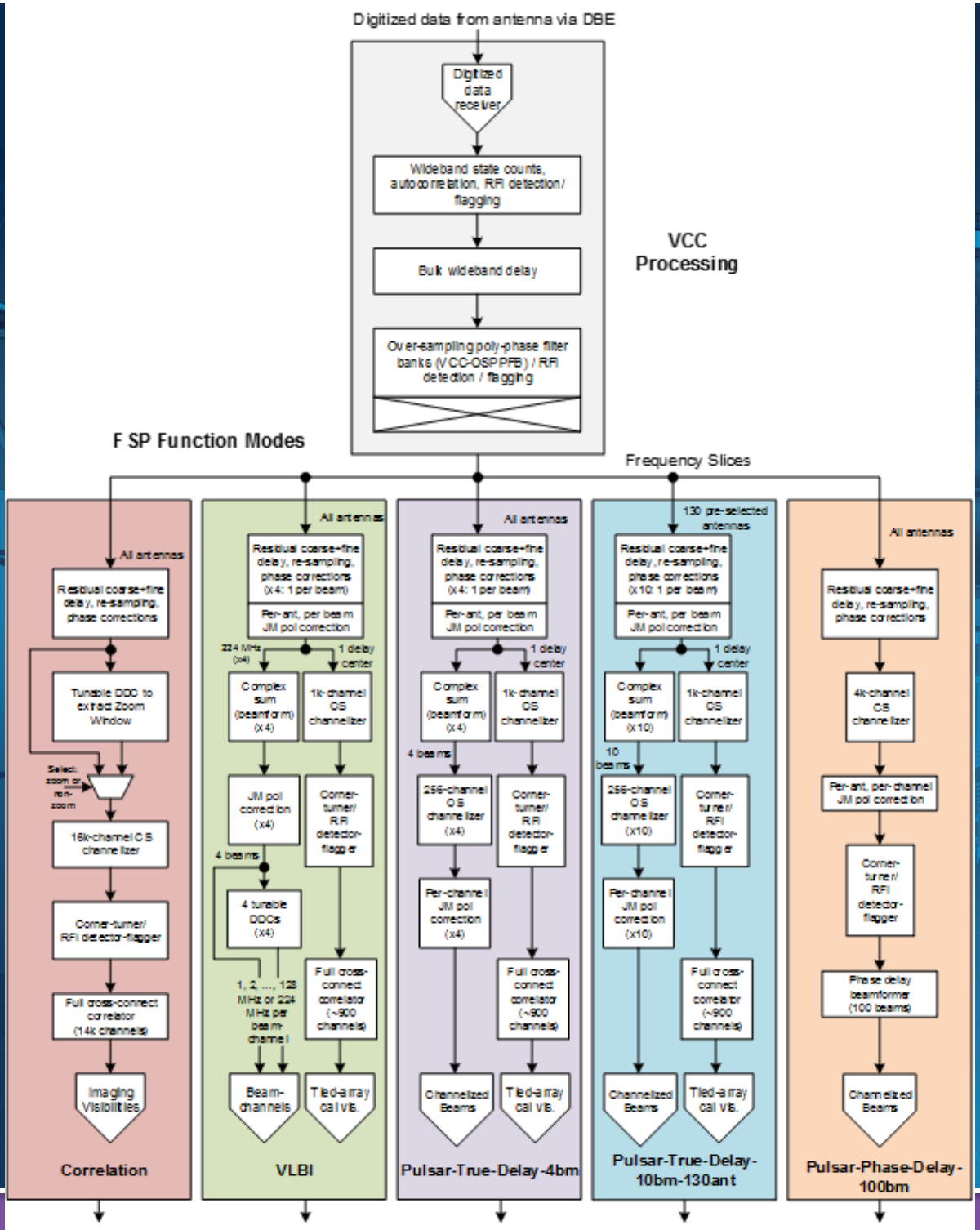
2U air-cooled TALON LRU prototype under test. Copper stacked-fin heatsinks would be replaced by liquid cooling plates for a 1U solution.

Trident-CBF Design

- Reference design for ngVLA CBF
- Leverages ~60 PYs of work on the SKA1 Mid.CBF
- FSA and TALON technology very well suited to the task, but ~2025 construction would at least use the next technology node
- High level design:
  - 3 “tridents” of 10 GHz/pol’n each
  - VCC-Part in each trident produces 50 Frequency Slices, processed in 50 FSPs – 150 FSPs in total
  - Each FSP can be one of: correlation for imaging, or 4 types of beamforming “Function Modes”

Trident-CBF Design




Digitized data from antenna via DBE
Digitized data receiver
Wideband state counts, autocorrelation, RFI detection / flagging
Bulk wideband delay
Over-sampling poly-phase filter banks (VCC-OSPPFB) / RFI detection / flagging
VCC Processing
F SP Function Modes
Frequency Slices
All antennas
Residual coarse+fine delay, re-sampling, phase corrections
Tunable DDC to extract Zoom Window
Select: zoom or non-zoom
16k-channel OS channelizer
Corner-turner/ RFI detector-flagger
Full cross-connect correlator (14k channels)
Imaging Visibilities
Correlation
Residual coarse+fine delay, re-sampling, phase corrections (x4: 1 per beam)
Per-ant, per beam JM pol correction
224 MHz (x4)
1 delay center
Complex sum (beamform) (x4)
1k-channel OS channelizer
JM pol correction (x4)
Corner-turner/ RFI detector-flagger
4 beams
4 tunable DDCs (x4)
1, 2, ..., 128 MHz or 224 MHz per beam-channel
Full cross-connect correlator (~900 channels)
Beam-channels
Tied-array cal vis.
VLBI
Residual coarse+fine delay, re-sampling, phase corrections (x4: 1 per beam)
Per-ant, per beam JM pol correction
1 delay center
Complex sum (beamform) (x4)
1k-channel OS channelizer
4 beams
256-channel OS channelizer (x4)
Corner-turner/ RFI detector-flagger
Per-channel JM pol correction (x4)
Full cross-connect correlator (~900 channels)
Channelized Beams
Tied-array cal vis.
Pulsar-True-Delay-4bm
130 pre-selected antennas
Residual coarse+fine delay, re-sampling, phase corrections (x10: 1 per beam)
Per-ant, per beam JM pol correction
1 delay center
Complex sum (beamform) (x10)
1k-channel OS channelizer
10 beams
256-channel OS channelizer (x10)
Corner-turner/ RFI detector-flagger
Per-channel JM pol correction (x10)
Full cross-connect correlator (~900 channels)
Channelized Beams
Tied-array cal vis.
Pulsar-True-Delay-10bm-130ant
Residual coarse+fine delay, re-sampling, phase corrections
4k-channel OS channelizer
Per-ant, per-channel JM pol correction
Corner-turner/ RFI detector-flagger
Phase delay beamformer (100 beams)
Channelized Beams
Pulsar-Phase-Delay-100bm
Data to archive via external switch

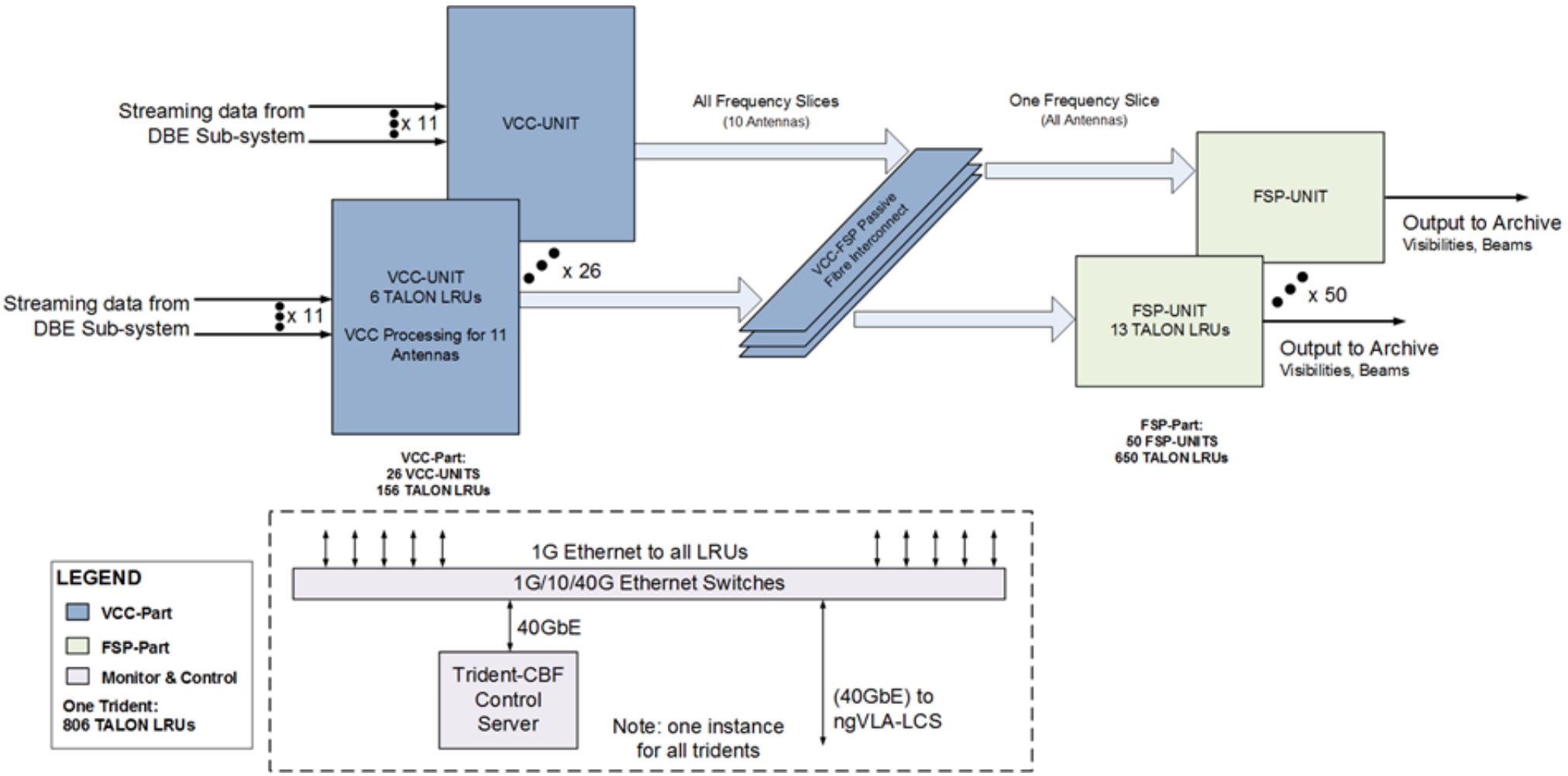
Trident-CBF Design

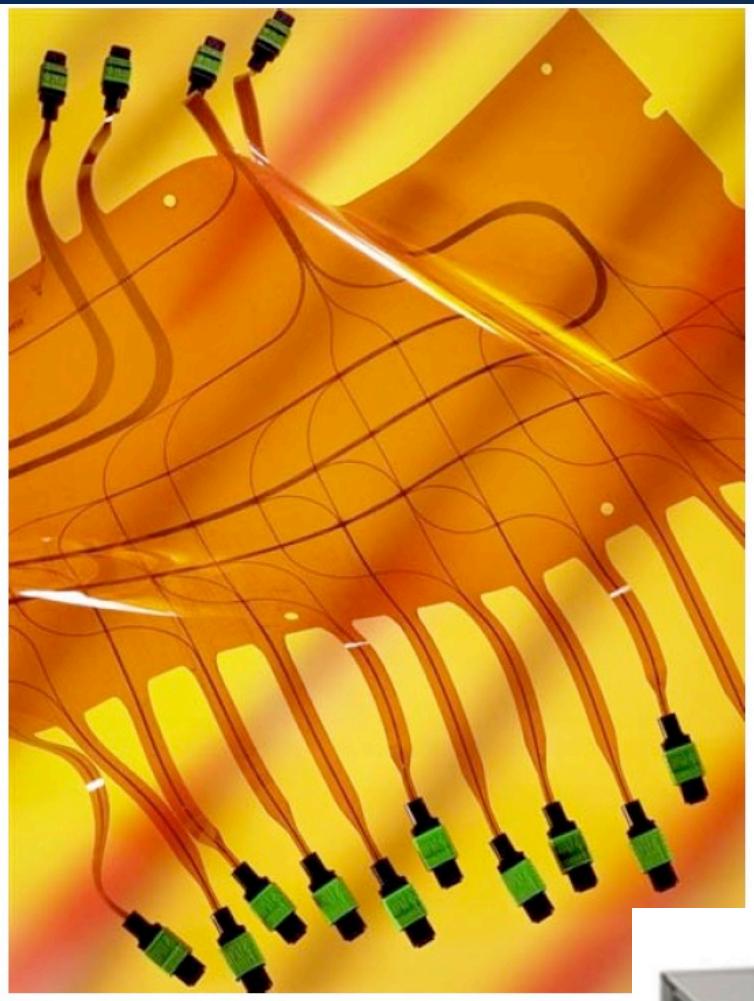
- The “VCC-UNIT” is a convenient collection of TALON LRUs to allow for passive fiber routing of one Frequency Slice for 11 antennas in it, to a single output 12-fiber MTP connector

- The “FSP-UNIT” accepts 26 x 11-fiber MTPs into (for ngVLA) its 26 FPGAs

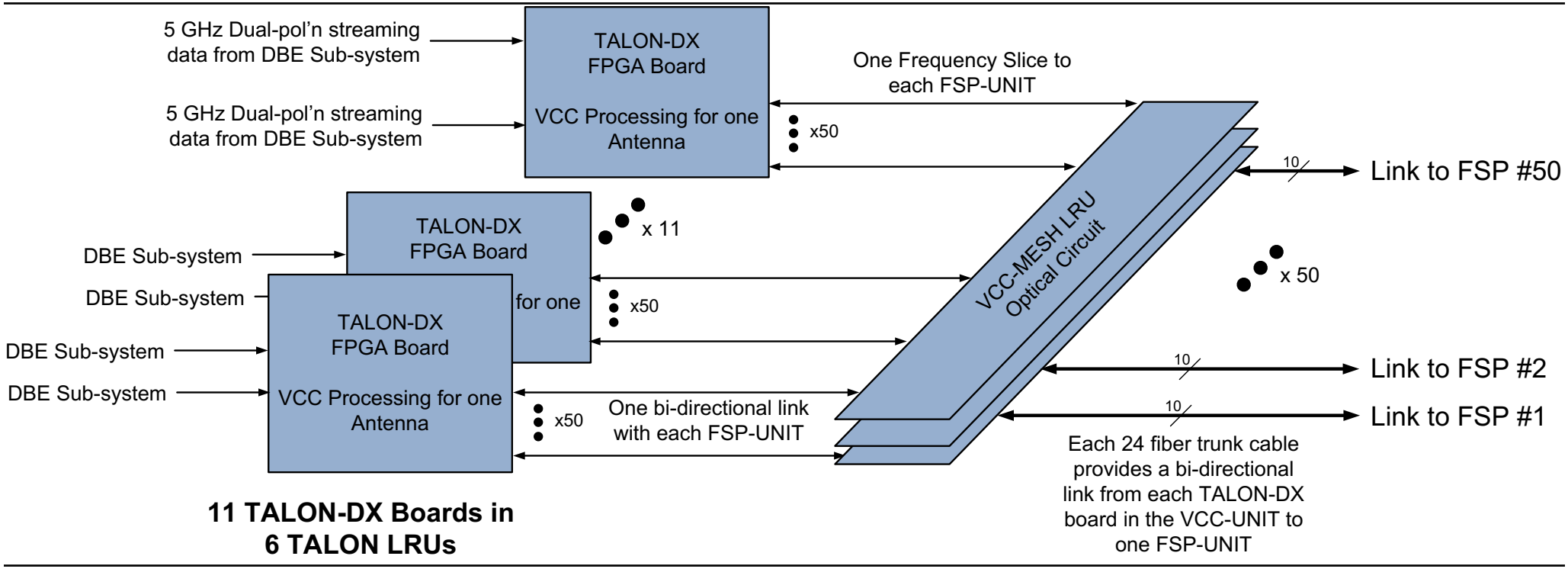
- The number of FPGAs in the FSP-UNIT can be increased if needed, for more antennas (up to 484) or for more processing horsepower

Trident-CBF Design -- Simplified Architecture



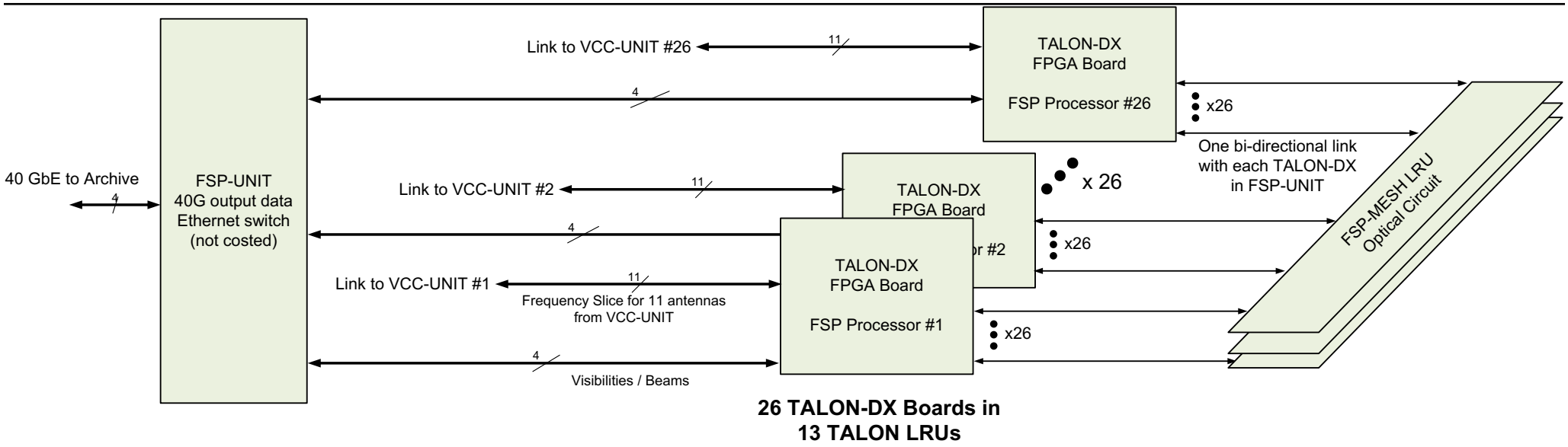


Trident-CBF Design -- VCC-Unit



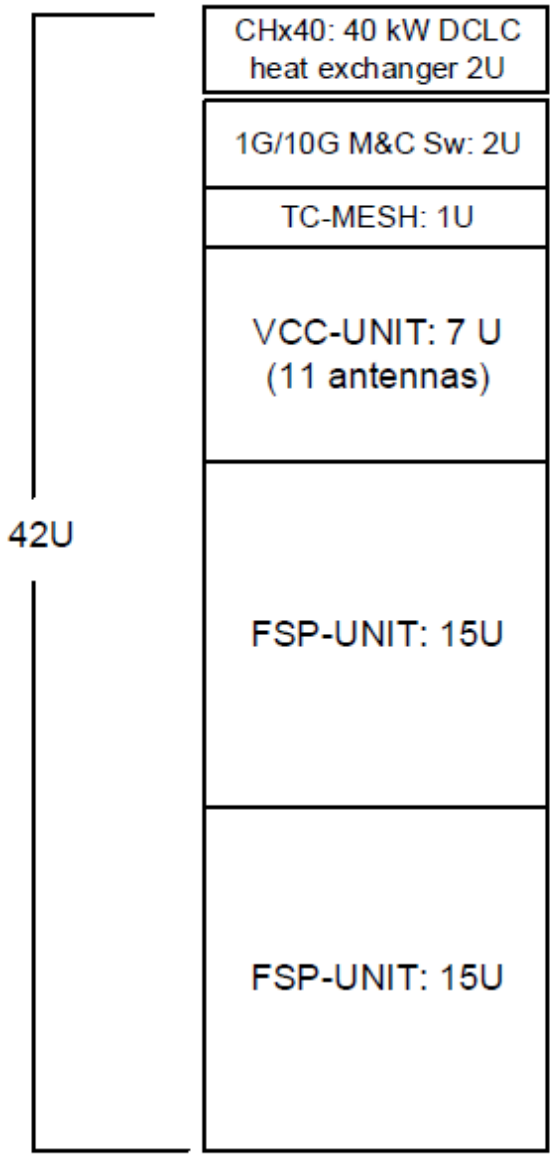
11 TALON-DX Boards in 6 TALON LRUs

Trident-CBF Design -- FSP-Unit



Trident-CBF Design -- Rack Layout

78 such racks in the entire Trident-CBF system…possibly a factor of 2 density improvement using 2025 technology.



Trident-CBF Design -- Cost Model

WBS Category Definition	WBS Category	Labour PDs									Total PDs	Labour PD%	Labour Cost	Non-Labour Cost	Travel Cost	Contingency	TOTAL COST
		PM:Sr	PM:Int	Eng:Sr	Eng:Int	Eng:Jr	Sci:Sr	Sci:Int	Con	Admin							
		$1,100	$900	$1,000	$900	$750	$1,050	$850	$950	$500							
Management	MGT	825	0	660	550	0	0	0	209	825	3069	16.0%	$2,673,550	$0	$261,000	$293,455	$3,228,005
System Engineering	SE	0	0	917	766	0	0	0	0	0	1683	8.8%	$1,606,367	$0	$220,400	$182,677	$2,009,443
Product Design	PD	0	0	0	0	0	0	0	0	0	0	0.0%	$0	$0	$0	$0	$0
Hardware Development	HW	0	0	0	606	0	0	0	0	0	606	3.2%	$545,738	$449,893	$69,600	$228,319	$1,293,550
Firmware Development	FW	0	0	0	4937	0	0	0	0	0	4937	25.8%	$4,443,683	$360,000	$208,800	$1,282,535	$6,295,018
Software Development	SW	0	0	0	3986	0	0	0	0	0	3986	20.8%	$3,587,704	$240,000	$139,200	$731,197	$4,698,101
Sub-System Integration Infrastructure	SII	0	0	88	461	0	0	0	0	0	549	2.9%	$502,975	$291,668	$34,400	$118,332	$947,376
Integration & Test (a.k.a. Development Testing)	I&T	0	0	193	1348	0	0	99	0	0	1639	8.6%	$1,489,400	$0	$413,800	$420,456	$2,323,656
Acceptance Test for Verification	AT	0	0	88	807	0	0	0	0	0	895	4.7%	$814,000	$116,006	$116,000	$83,680	$1,129,686
Shipping and Installation	S&I	0	0	0	128	0	0	0	0	293	422	2.2%	$262,167	$160,000	$60,200	$42,589	$524,956
Procurement and Production Hardware Cost	PHW	0	110	0	0	231	0	0	0	110	451	2.4%	$327,250	$91,763,078	$46,400	$9,205,200	$101,341,928
Warranty	WTY	41	6	102	692	12	0	5	10	61	929	4.8%	$828,392	$4,669,032	$83,710	$631,618	$6,212,752
TOTALS		**866**	**116**	**2047**	**14282**	**243**	**0**	**104**	**219**	**1290**	**19166**	**100.0%**	**$17,081,224**	**$98,049,677**	**$1,653,510**	**$13,220,059**	**$130,004,469**

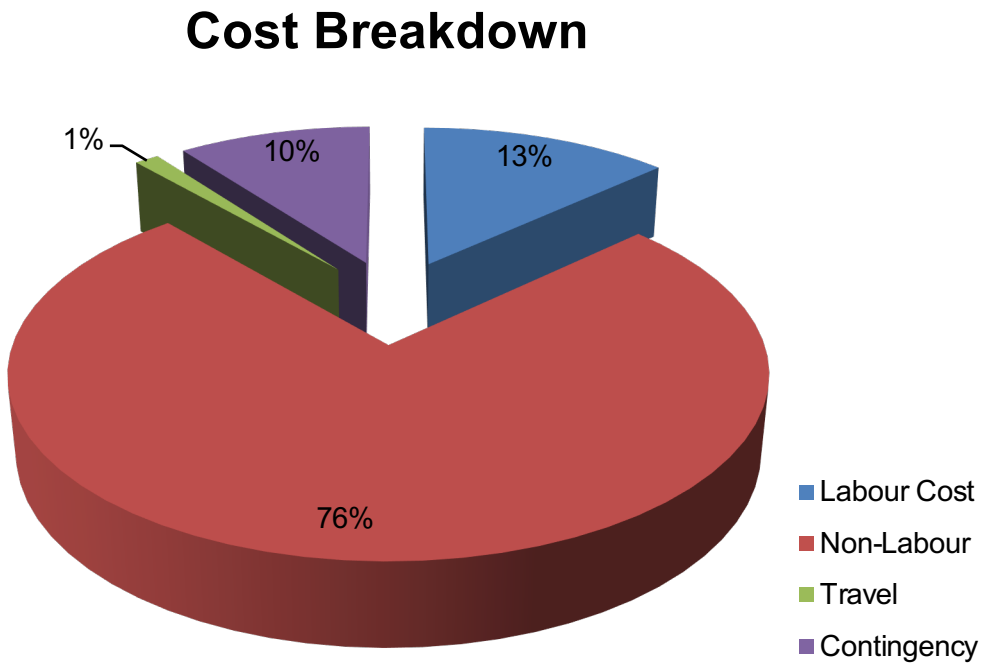
Figure 13-1 Trident-CBF cost summary, based on the SKA1 Mid.CBF cost model, 2018 dollars. This is for 6 TALON LRUs per VCC-UNIT, 24 VCC-UNITs, and 13 TALON LRUs per FSP-UNIT.

WBS Category Definition	WBS Category	Labour PDs									Total PDs	Labour PD%	Labour Cost	Non-Labour Cost	Travel Cost	Contingency	TOTAL COST
		PM:Sr	PM:Int	Eng:Sr	Eng:Int	Eng:Jr	Sci:Sr	Sci:Int	Con	Admin							
		$1,100	$900	$1,000	$900	$750	$1,050	$850	$950	$500							
Management	MGT	825	0	660	550	0	0	0	209	825	3069	16.0%	$2,673,550	$0	$261,000	$293,455	$3,228,005
System Engineering	SE	0	0	917	766	0	0	0	0	0	1683	8.8%	$1,606,367	$0	$220,400	$182,677	$2,009,443
Product Design	PD	0	0	0	0	0	0	0	0	0	0	0.0%	$0	$0	$0	$0	$0
Hardware Development	HW	0	0	0	606	0	0	0	0	0	606	3.2%	$545,738	$449,893	$69,600	$228,319	$1,293,550
Firmware Development	FW	0	0	0	4937	0	0	0	0	0	4937	25.8%	$4,443,683	$360,000	$208,800	$1,282,535	$6,295,018
Software Development	SW	0	0	0	3986	0	0	0	0	0	3986	20.8%	$3,587,704	$240,000	$139,200	$731,197	$4,698,101
Sub-System Integration Infrastructure	SII	0	0	88	461	0	0	0	0	0	549	2.9%	$502,975	$291,668	$34,400	$118,332	$947,376
Integration & Test (a.k.a. Development Testing)	I&T	0	0	193	1348	0	0	99	0	0	1639	8.6%	$1,489,400	$0	$413,800	$420,456	$2,323,656
Acceptance Test for Verification	AT	0	0	88	807	0	0	0	0	0	895	4.7%	$814,000	$116,006	$116,000	$83,680	$1,129,686
Shipping and Installation	S&I	0	0	0	128	0	0	0	0	293	422	2.2%	$262,167	$160,000	$60,200	$42,589	$524,956
Procurement and Production Hardware Cost	PHW	0	110	0	0	231	0	0	0	110	451	2.4%	$327,250	$96,647,568	$46,400	$9,693,649	$106,714,867
Warranty	WTY	41	6	102	692	12	0	5	10	61	929	4.8%	$828,392	$4,913,257	$83,710	$656,040	$6,481,399
TOTALS		**866**	**116**	**2047**	**14282**	**243**	**0**	**104**	**219**	**1290**	**19166**	**100.0%**	**$17,081,224**	**$103,178,392**	**$1,653,510**	**$13,732,930**	**$135,646,056**

Figure 13-2 Trident-CBF cost summary (2018 dollars) for the 5 TALON LRUs per VCC-UNIT, 28 VCC-UNITs, and 14 TALON LRUs per FSP-UNIT option mentioned as a note to Figure 5-1.

Trident-CBF Design -- Cost and Power

- Current FPGA Technology:
  - $130 Million (2018 USD)
    - $90M Hardware Costs
    - $17M Labor
    - $13M Contingency
  - Power Estimate: 1500 kW



- Next Generation FPGA Technology (Estimated):
  - $108M-$121M respectively (2018 USD)
  - 900 – 1200 kW

Thank you

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