ALMA Digital Downconverter

Sylas Ashton

National Radio Astronomy Observatory

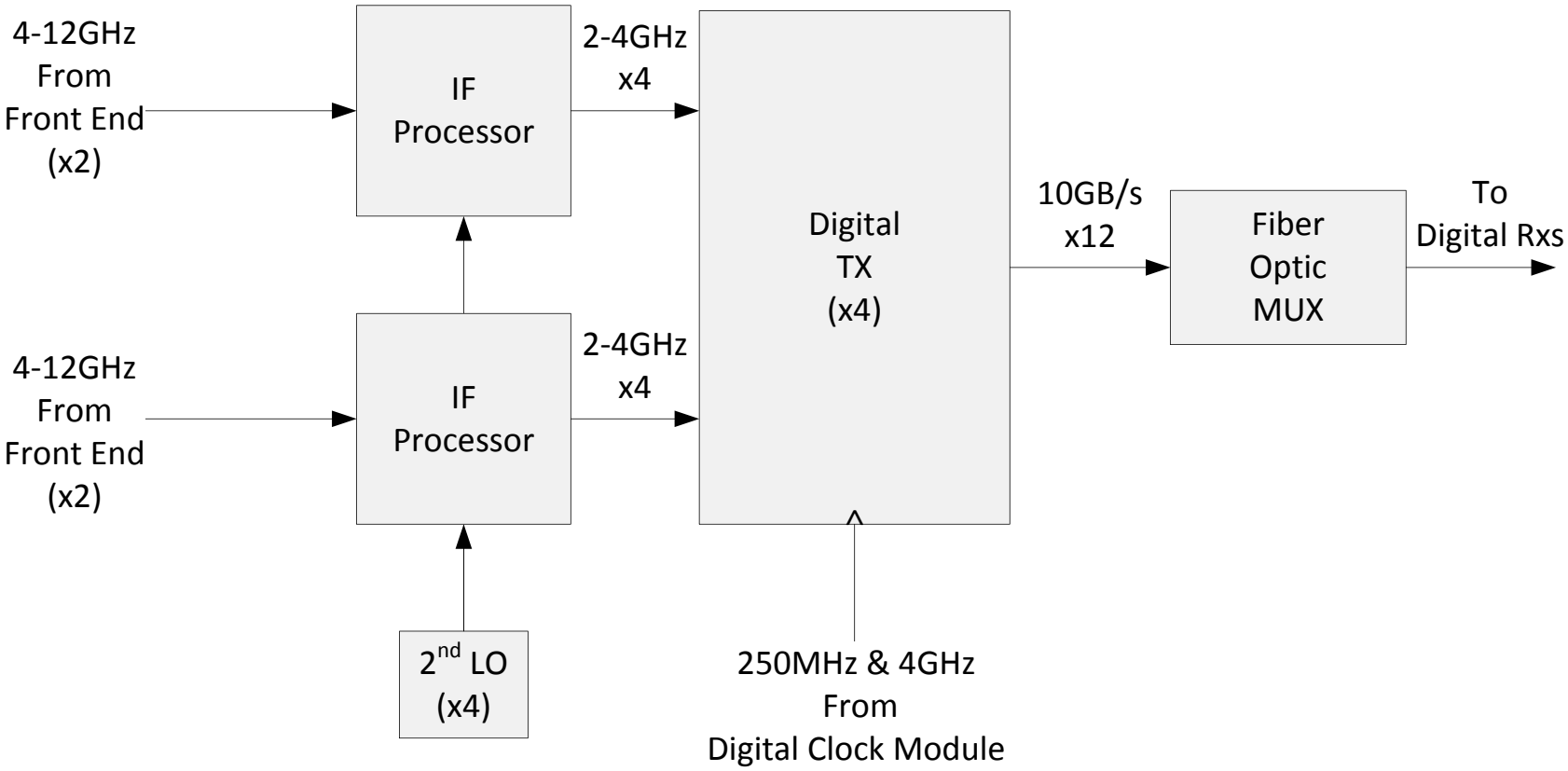
Outline

- Goals
- Block Diagram
- ADC
- FPGA
- Data Transmission
- Monitor and Control
- Alternate Uses

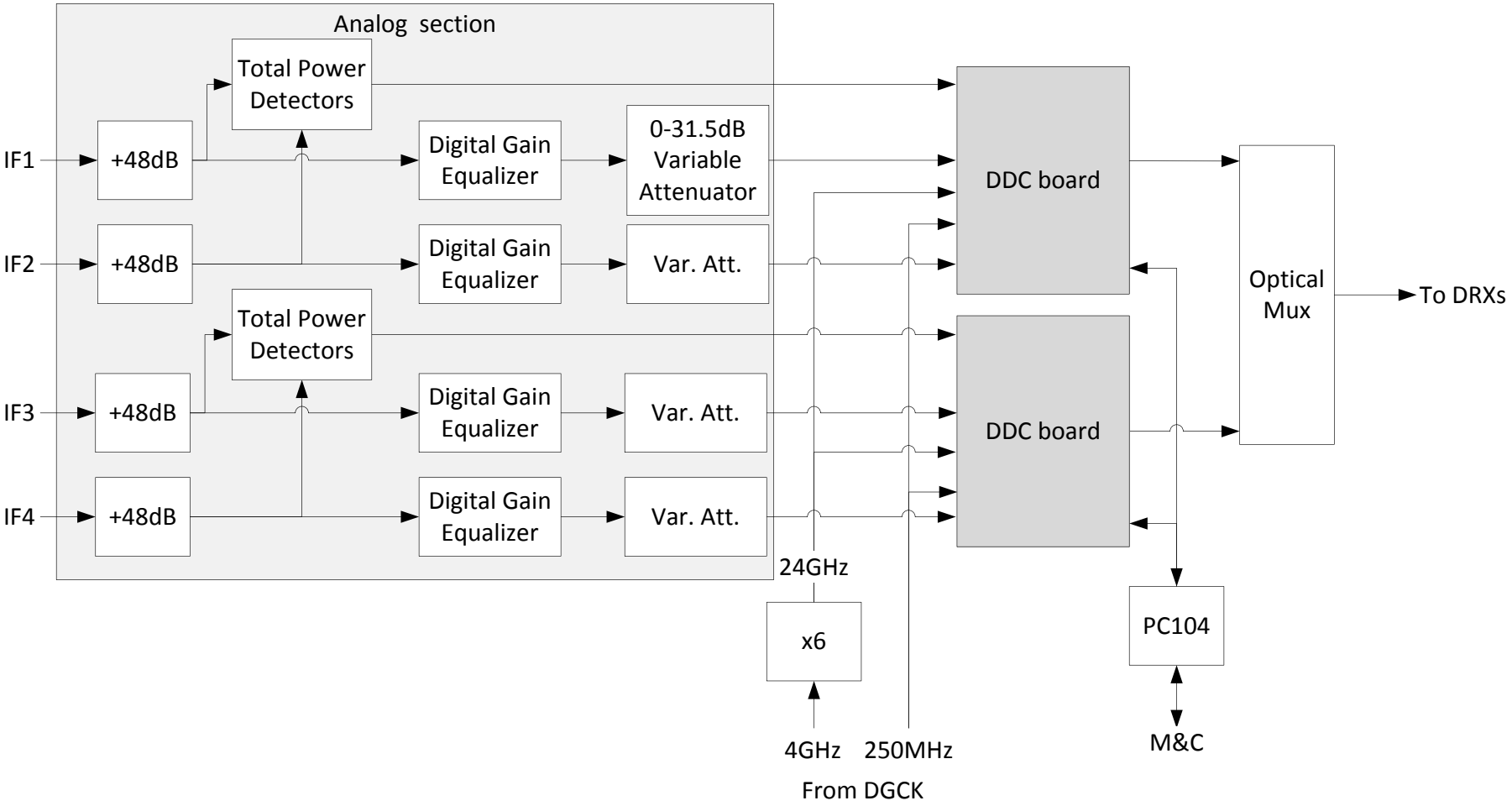
Goals

- Directly sample the ALMA IF, 4 to12GHz
- Digitally downconvert to basebands of 2 to 4GHz
- Transmit basebands to Digital RXs
- Be compatible with expected double data rate correlator upgrade
  - Basebands of 4 to 8GHz
  - 240Gb/s over single fiber

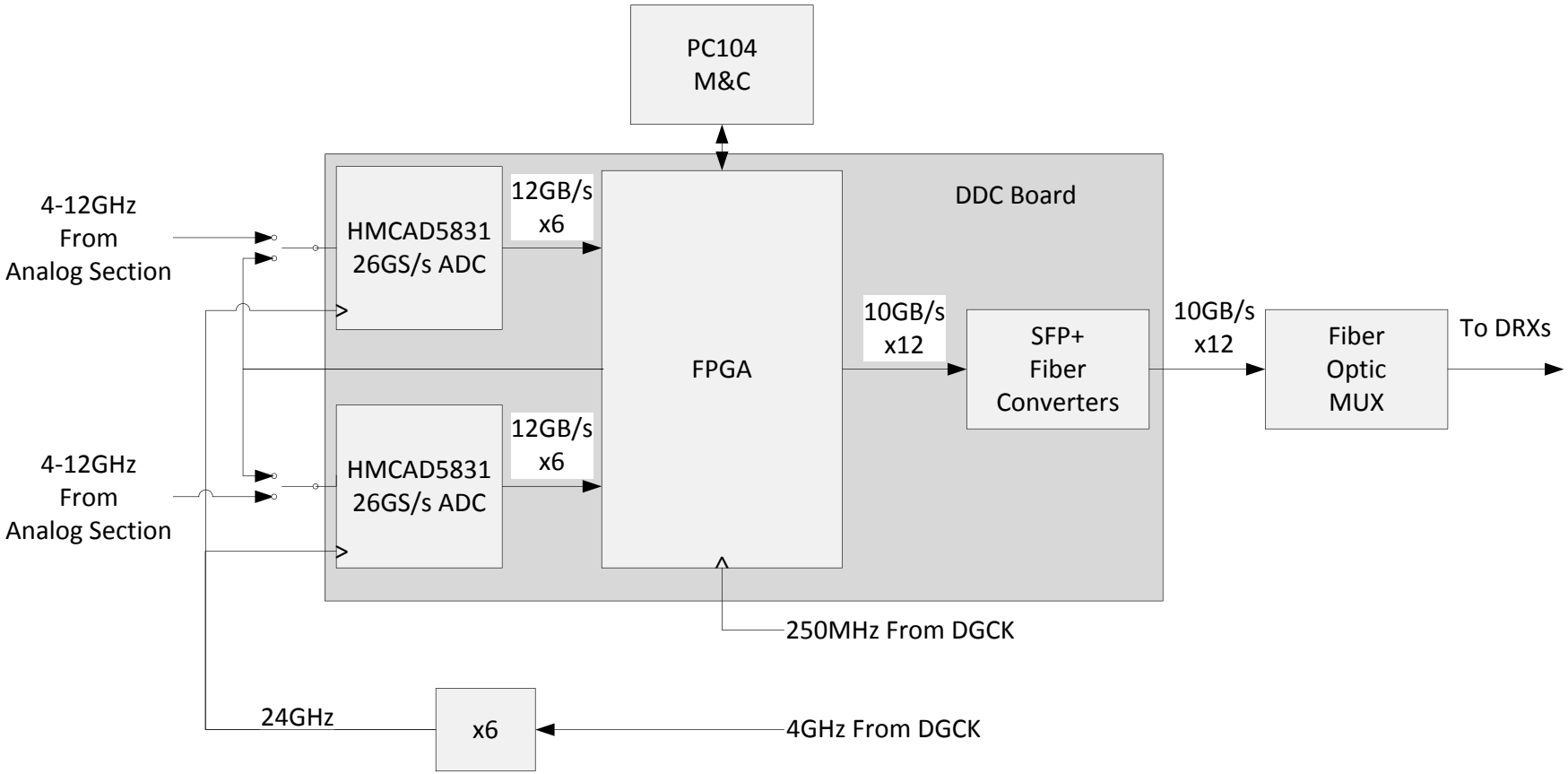
Block Diagram – Current System



Block Diagram

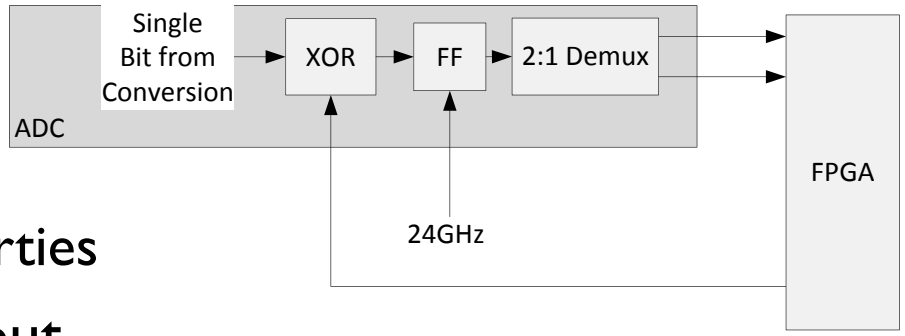


DDC Board Block Diagram

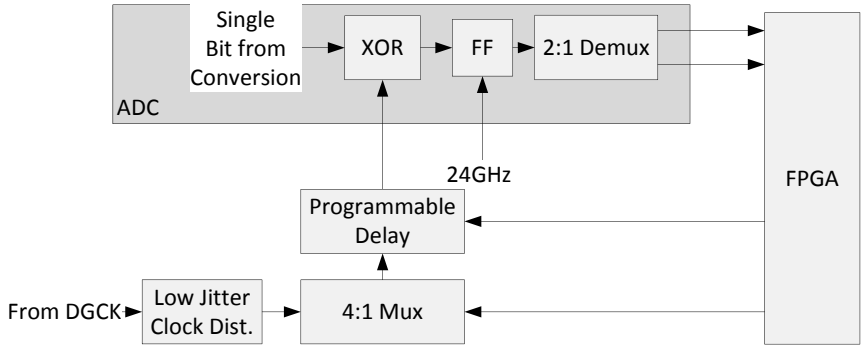


ADC Interface

- FPGA with multiple 12Gb/s transceivers
- XOR bit pattern
  - Needs to be external to ADC
  - Low Jitter
  - Adjustable delay
  - Zero DC
  - Strong autocorrelation properties
- Pattern generator for ADC input
  - Aligns data from ADC to system clock



XOR pattern generator



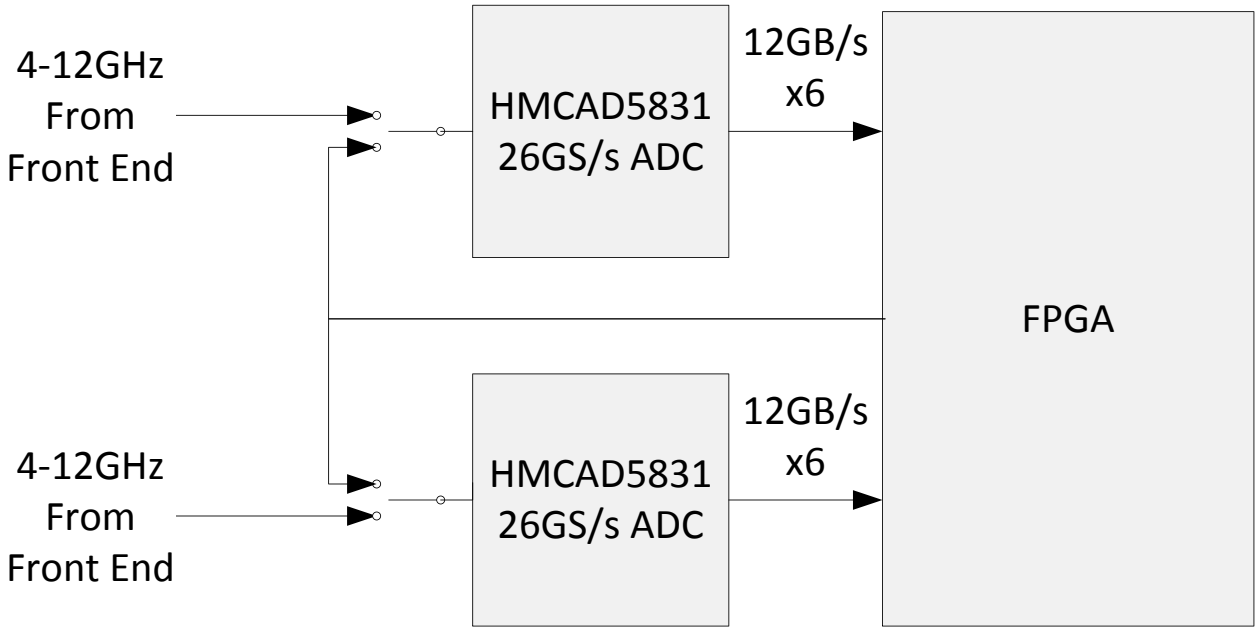
- HMC856 Delay circuit
  - 3ps delay resolution
- HMC847 36Gbs MUX
  - Lower jitter than FPGA transceivers
  - Re-clocks FPGA data with 250MHz from DGCK
- SY58608U low jitter fan-out buffers
  - 250MHz distribution
- Complementary Sequence
  - Can be made with zero DC at the ADC and to the MUX
  - Good autocorrelation properties

XOR Input Jitter

- 4.92 ps Total Expected Jitter, <12% of 1 cycle @24GHz
  - 0.56 ps from each DGCK clock
  - 0.13 ps from each 250MHz fan-out buffer
  - 4.25 ps from MUX
  - 2.2 ps from phase shifter
- FPGA transmitter jitter ~60% of 1 cycle @24GHz
  - Designed for 13Gb/s operation
  - Timing may work with next gen. 30Gb/s transceivers

ADC input pattern generator

- Single IO line from the FPGA
- Off board RF switches
- Used in EVLA design at 4GHz

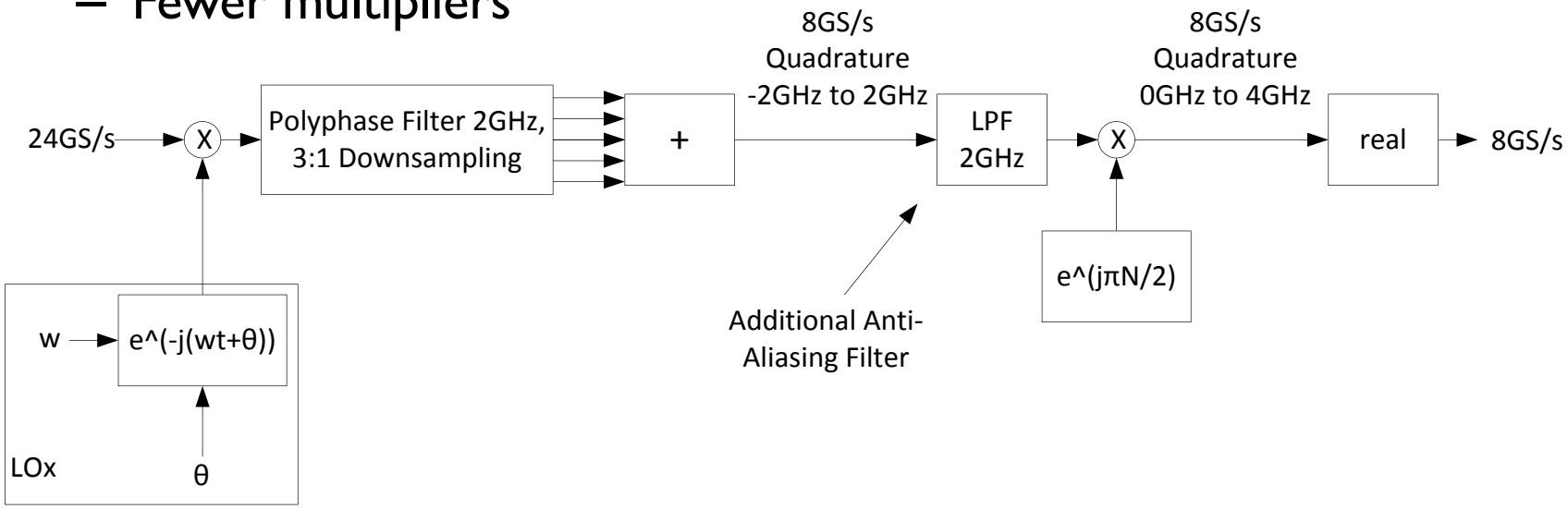


FPGA

- Kintex 7 Ultrascale KU115
- 5520 DSP blocks
- 52 13Gb/s Transceivers
  - 24 to SFP+ @10Gb/s
  - 12 to ADCs @12Gb/s

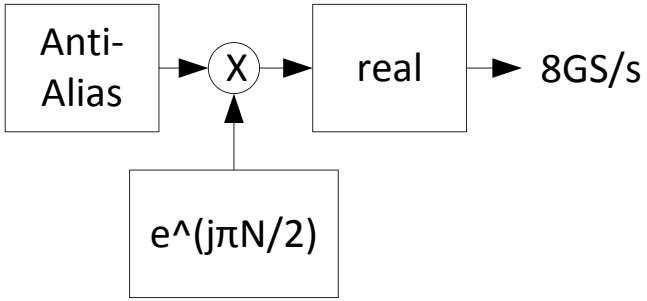
Downconverter

- Frequency shift by complex LO
- Polyphase filter for downsampling
  - Processes at 8GHz
  - Filters at 24GHz
- Anti-Alias at 8GHz
  - Fewer multipliers



DSP

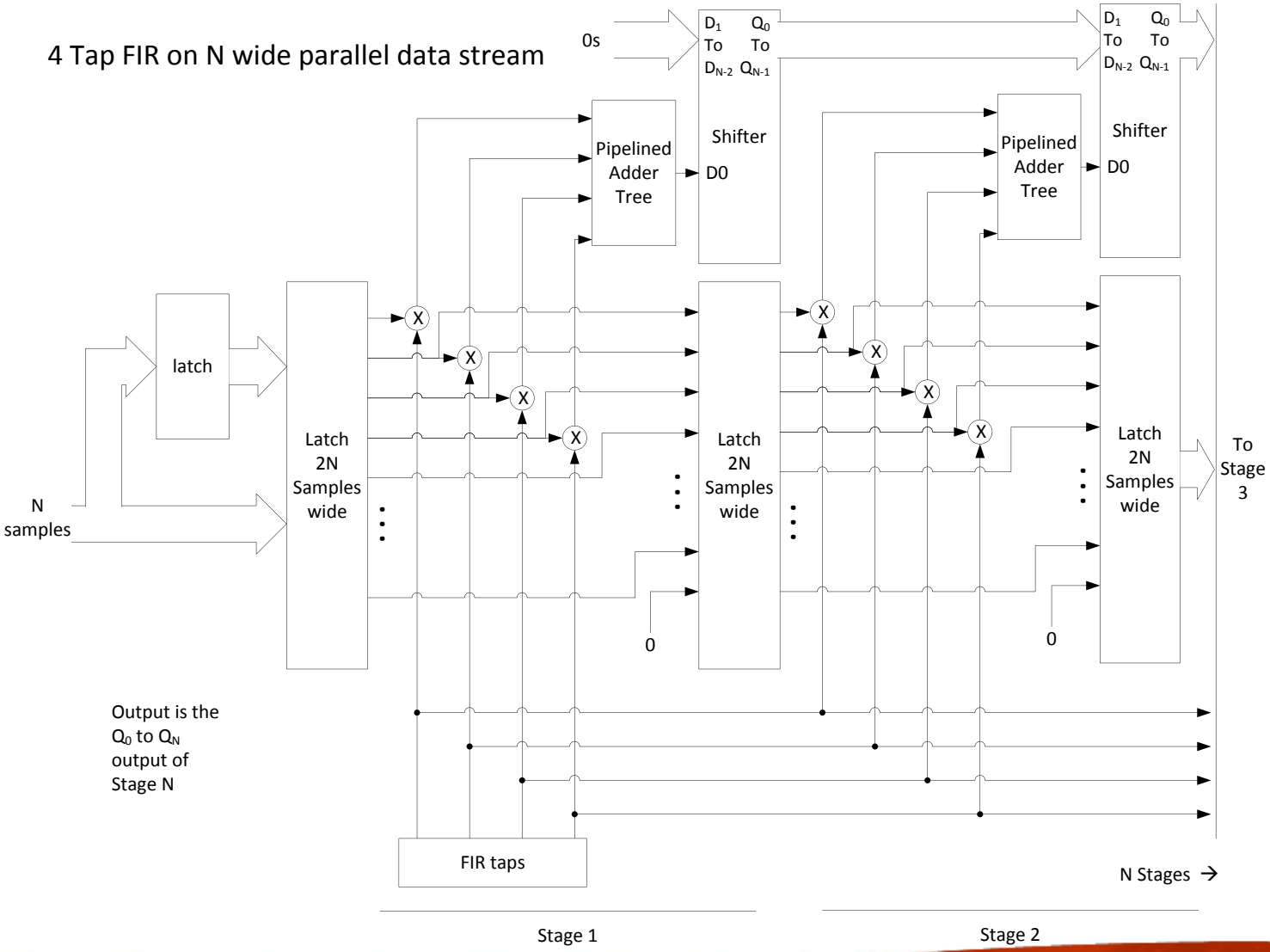
- DSP at 8GHz
  - FPGA clock is 400MHz
  - 20 Stage pipelining
- Find minimum DSP usage to meet filtering goals
- Third band filter as polyphase filter prototype
  - 21 tap filter using 15 multipliers
- Half band filter as anti-alias filter
  - Half of filter taps are zero
  - Pre-add symmetric tap terms
  - Half of the outputs aren't used
  - 45 tap filter using 6 multipliers



FIR filter block

- Fully Parameterized
  - Number of taps
  - Number of pipeline stages
  - Bit width
  - Pre-add option for symmetric filters

FIR filter


4 Tap FIR on N wide parallel data stream
0s
D1 Q0
To To
DN-2 QN-1
Shifter
D0
Pipelined Adder Tree
latch
N samples
Latch 2N Samples wide
X
0
Output is the Q0 to QN output of Stage N
FIR taps
To Stage 3
N Stages
Stage 1
Stage 2

Data Transmission

- ALMA time multiplexes 2 data streams onto a three wavelength link.
- Make use of current ALMA Digital RXs for testing
- Use FPGA transceivers with 10Gb/s SFP+ transmitters
  - Compact
  - Inexpensive
  - Low power
- 24:1 optical mux

Monitor & Control

- PC104 board
  - Linux
  - ISA bus
  - 1GbE
- Good bandwidth to FPGA
- Gets away from CAN
- Remote reloading of FPGA
  - Used in EVLA correlator
- Power supply sequencing
- EEPROM always readable

Alternate Uses

- Wideband, single IF Water Vapor Radiometer
- ngVLA test platform
  - Directly sample C and X bands
  - Directly sample Ku band in 2nd Nyquist
  - K,Ka or Q through a single downconverter
- Any broadband back end
  - If it has a flat gain slope across input bandwidth
- Inline data stream processor
  - e.g. RFI filtering for 8 bit samplers

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